Application Note SIlicon Capacitor

Lifetime of 3D Capacitors in Murata technologies

Rev 3.4

Introduction

The 3D Murata technologies provide several passive components including High Density Capacitors.

The lifetime of those 3D Silicon Capacitors has been determined using accelerated lifetime tests.

The Time-Dependent Dielectric Breakdown (TDDB) measurements are used to model the intrinsic behavior of the capacitor dielectric under elevated temperature and strong electric field. The acceleration factors for temperature and electric field are used to extrapolate the capacitor lifetime under typical operating conditions.

The Temperature Cycling (TMCL) tests are done to assess the endurance of non-hermetic packaged solid-state devices exposed to thermo-mechanical stress as a result of expansion and contraction by high and low temperature.

Summary

Lifetime for 3D-capacitor in Murata technology :

- PICS3 (BV11) is higher than 10 years @ 3.6V
- PICS1 is higher than 10 years @ 5.5V
- PICSHV150 (BV150) is higher than 10 years @ 68V
- PICS3HV (BV30) is higher than 10 years @ 16V
- PICSHV50 (BV50) is higher than 10 years @ 21V
- PICSHV100 (BV100) is higher than 10 years @ 32V

Thermo-mechanical lifetime for Murata technology:

- PICS3 (BV11) is higher than 10 years in Telecom Hand Held use conditions
- PICS3CR (BV11) is 23 years in Telecom Hand Held use conditions

Key applications

- Stand alone IPD components
- System-in-Package (SiP) interposer
- Companion chip

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3D capacitor lifetime

3D-capacitor description

3D-capacitor consists of a MOS structure (Metal Oxide Semiconductor) as presented on Figure 1. The dielectric stack is grown on the 3D silicon substrate as lower electrode. The top electrode of the device is made of polysilicon and aluminum metal.

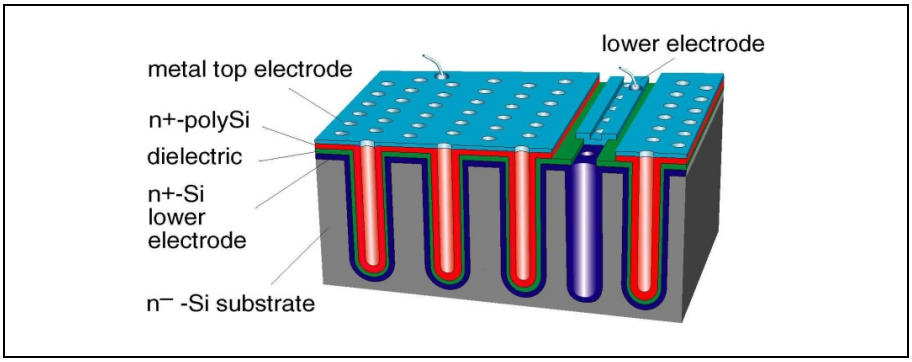

Figure 1: Description of 3D-capacitor structure

When dielectrics, such as silicon dioxide, are stored at fixed voltage and temperature, breakdown is observed after time. This Time-Dependent Dielectric Breakdown (TDDB) is a known failure mode in integrated circuits. Intrinsic breakdowns occur in oxides that are free of defects when the inherent, intrinsic tolerances of the dielectric material wear out. Wear out is accelerated under high voltage or high temperature conditions.

Dielectric-breakdown testing: constant voltage

In constant-voltage tests the oxide is exposed to higher than designed operating voltages, and the time to breakdown is measured. To completely characterize dielectric life, TDDB tests are generally conducted to span a desired matrix of electric field and temperature values. The E-model is supported by published data and widely used down to 4nm, according to JEDEC standard (JP001.01 – May 2004). The Time To Failure (TTF) relates to the electric field (E_{ox}) as Equation (1) shows:

$$TTF \propto e^{-\gamma E_{ox}} . e^{E_a/kT} \quad (1)$$

with γ = field acceleration factor

E_a = activation energy

k = Boltzmann's constant

The electric field E_{ox} is given by the ratio of the applied stress voltage (V_g) to thickness of the dielectric layer. For a given temperature, a simplified model can be used as is shown in Equation (2):

$$TTF \propto e^{-MV_g} \quad (2)$$

where M (voltage acceleration factor) is a constant proportional to γ. Thus, using Equation (2), the E-model predicts that the relation is exponential, or, if TTF is plotted on the y-axis using a log scale and V_g on the x-axis using a linear scale, the relation is linear on such a plot, where M is the slope of the line.

This line is extrapolated to the operating voltage for lifetime prediction.

Test methodology

TDDB measurements are run at wafer level with a minimum of 2 lots and 2 wafers per lot. At least 8 DUT (Device Under Test) per wafer are evaluated, for every stress condition (voltage and temperature combination).

Figure 2 shows a procedure for the constant voltage stress (CVS) method.

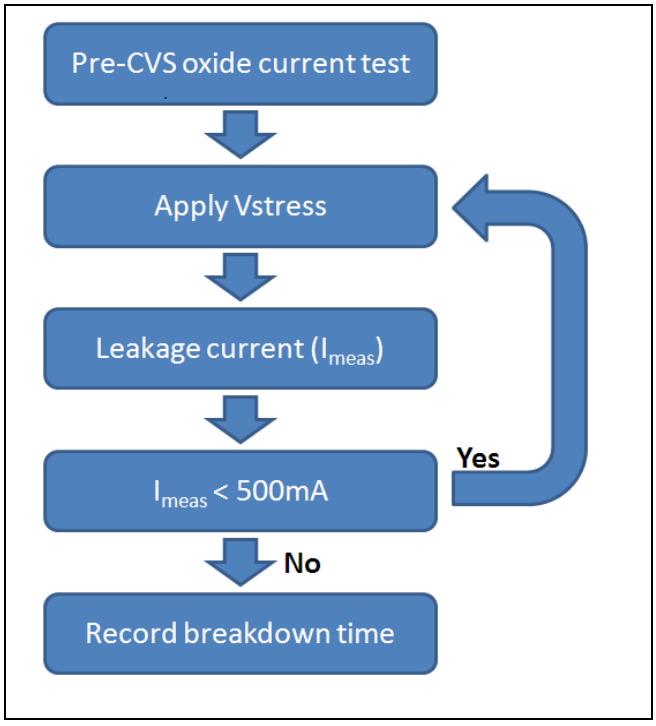

Figure 2: Test flow diagram

Pre-CVS is performed for identifying initial failed samples. The leakage current is measured at the applied use voltage. If the measured current is larger than the defined criterion, then, that sample is rejected as an initial failed sample.

Experimental results

TDDB E-model predictions

It is believed that oxide breakdown can be described as “weakest link” statistics described by Weibull distribution. The raw data is statistically analyzed using a linearized Weibull plot to determine Time To Failure extrapolated down to 0.1% cumulative failures (t0.1%). The extrapolated t0.1% is plotted against test voltage in Figure 3, with 60% Confidence Level (60% C.I.) intervals.

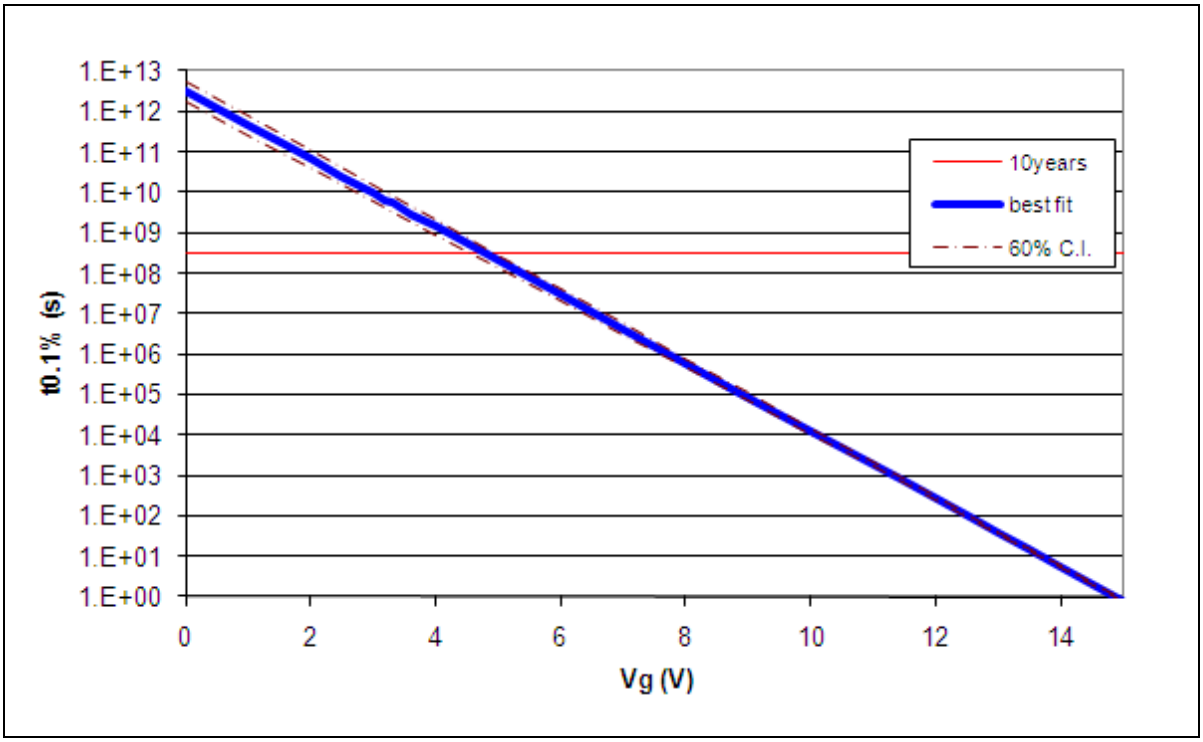

Figure 3: Lifetime predictions for 3D-capacitors under 100°C

Intrinsic lifetime for 3D-capacitors is 60 years, with nominal dielectric thickness at 100°C, for PICS3 (BV11) technology at 3.6V.

Influence of temperature

TDDB measurements were run at 3 temperatures, up to 150°C, in order to determine the Arrhenius acceleration model presented in Equation (1). Capacitor lifetimes with nominal dielectric thickness at 37°C, 100°C, 150°C and 225°C are presented in Figure 4.

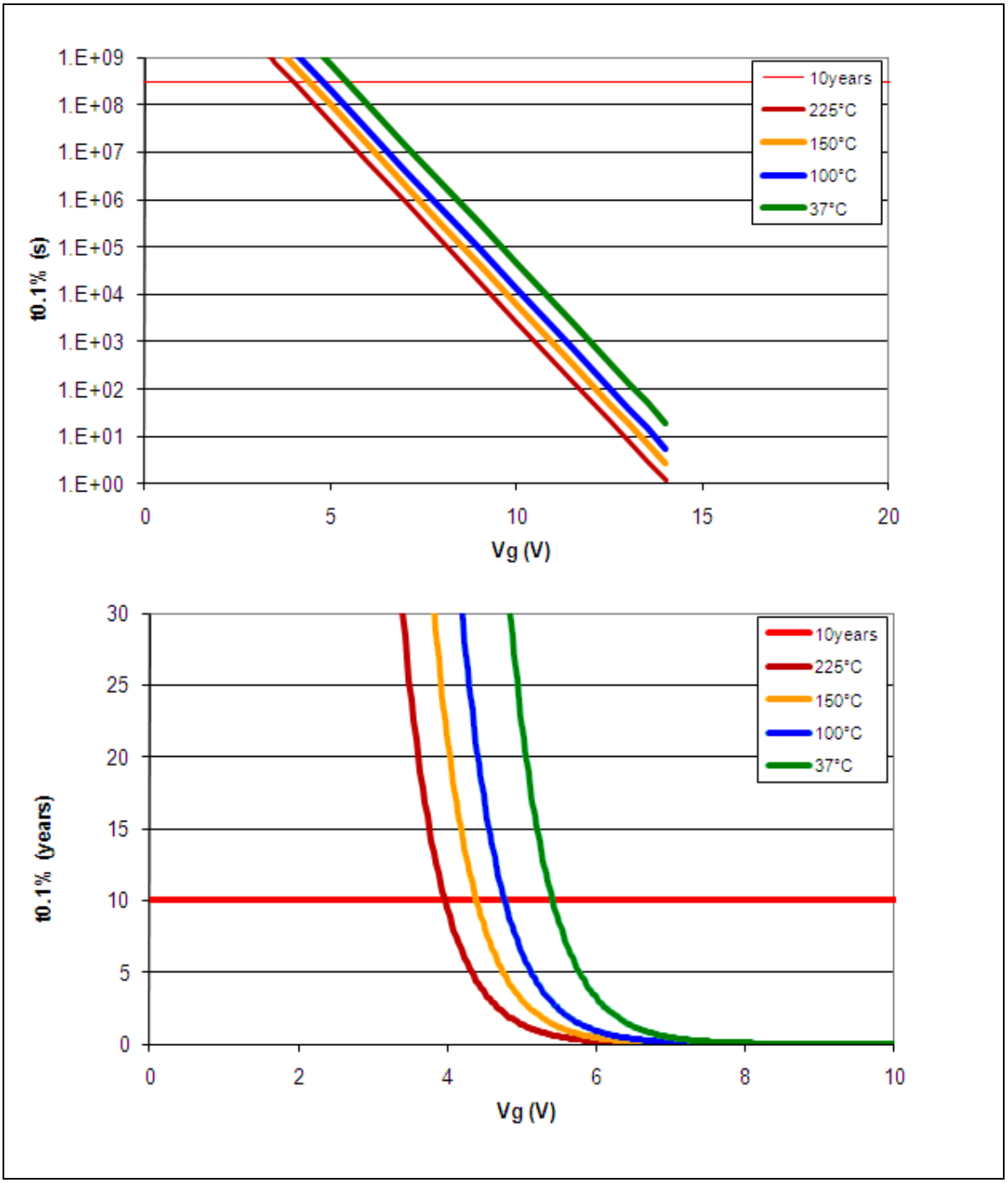

Figure 4: Lifetime predictions for 3D-capacitors under 4 different temperatures in logarithmic scale (top) and linear (bottom)

Figure 5 illustrates the influence of temperature on capacitor lifetime with nominal dielectric thickness at 3.6V, 4.5V, 5V and 7V.

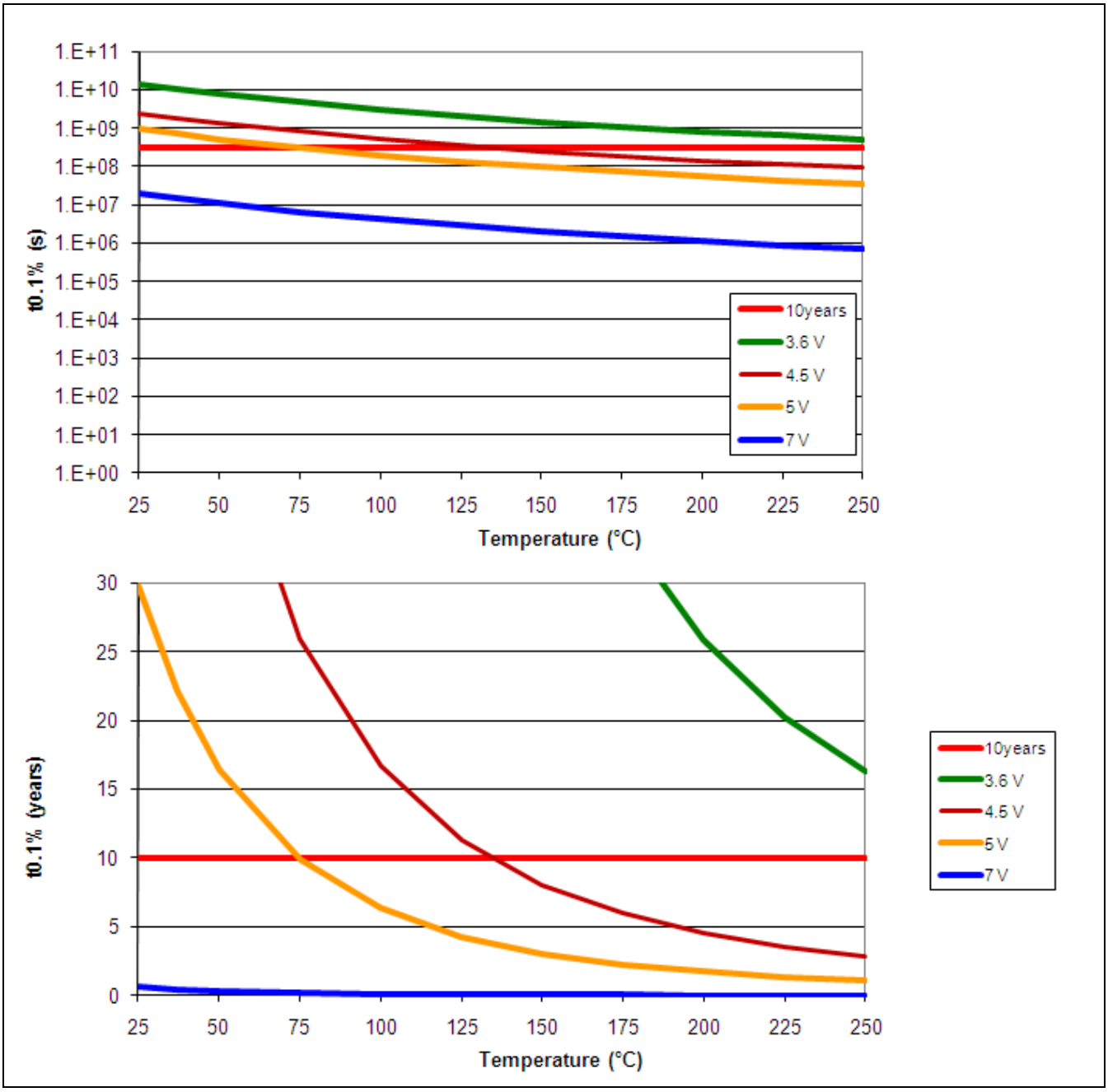

Figure 5: Lifetime predictions for 3D-capacitors under 4 different voltages in logarithmic scale (top) and linear scale (bottom)

Influence of dielectric thickness

Due to process variations, the dielectric thickness may vary. Thinner dielectric involves higher electric field, lower breakdown voltage and shorter capacitor lifetime. TDDB results in Figure 6 are dedicated to the lifetime for 2 dielectric thicknesses: nominal thickness and minimum thickness within production limits.

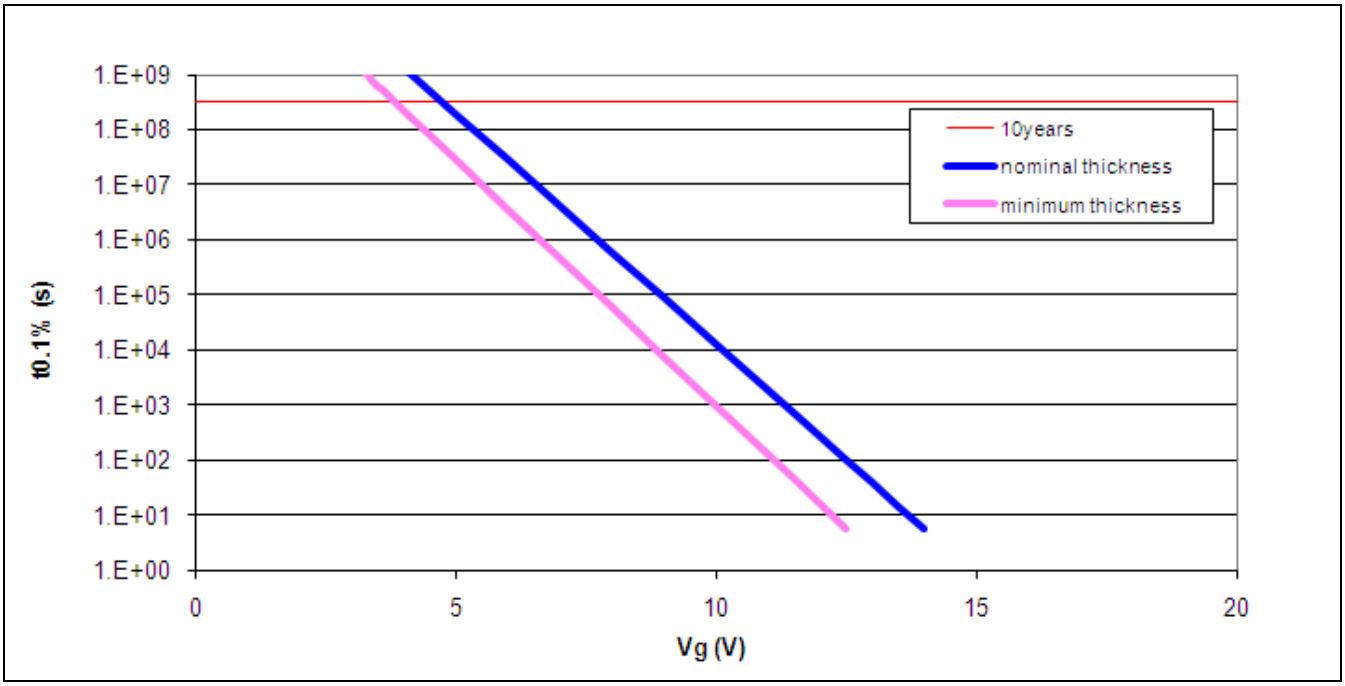

Figure 6: Influence of dielectric thickness on lifetime at 100°C

Intrinsic lifetime versus temperature & operating voltage

Table 1 summarizes the lifetime predictions at different values of applied stress voltage (V_g) and temperatures, using the TDDB E-model at 0.1% cumulative failures, for PICS3 3D-capacitors (BV11) with the minimum dielectric thickness:

Vg (V)	37°C	100°C	150°C	225°C
3.6	57 years	16 years	8 years	4 years
4.5	9 years	2.6 years	1.3 years	202 days
5	3.2 years	338 days	163 days	72 days
7	19 days	5.5 days	2.7 days	28 hours

Table 1: Lifetime predictions based on TDDB E-model
(PICS3 capacitor (BV11) in Murata technology with minimum dielectric thickness)

Table 2 summarizes the lifetime predictions at different values of applied stress voltage (V_g) and temperatures, using the TDDB E-model at 0.1% cumulative failures, for PICS1 3D-capacitors with minimal dielectric thickness:

Vg (V)	37°C	100°C	150°C	225°C
5.5	31818 years	1353 years	215 years	27 years
7	5189 years	220 years	35 years	4 years
8.5	846 years	36 years	5 years	266 days
10	138 years	5 years	342 days	43 days

Table 2 Lifetime predictions based on TDDB E-models
(PICS1 capacitor (BV11) in Murata technology with minimal dielectric thickness)

Table 3 summarizes the lifetime predictions at different values of applied stress voltage (V_g) and temperatures, using the TDDB E-model at 0.1% cumulative failures, for PICSHV150 3D-capacitors (BV150) with minimal dielectric thickness:

Vg (V)	37°C	100°C	150°C	225°C
30	496676 years	36581 years	8022 years	1458 years
45	20090 years	1480 years	324 years	59 years
60	813 years	60 years	13 years	2.4 years
75	33 years	2.4 years	194 days	35 days

Table 3: Lifetime predictions based on TDDB E-model
(PICSHV150 capacitor (BV150) in Murata technology with minimal dielectric thickness)

Table 4 summarizes the lifetime predictions at different values of applied stress voltage (V_g) and temperatures, using the TDDB E-model at 0.1% cumulative failures, for PICS3HV 3D-capacitors (BV30) with minimal dielectric thickness:

Vg (V)	37°C	100°C	150°C	225°C
10	3076 years	671 years	276 years	102 years
13	377 years	82 years	33 years	12 years
16	46 years	10 years	4.1 years	1.5 years
19	5.6 years	1.2 years	186 days	69 days

Table 4: lifetime predictions based on TDDB E-model
(PICS3HV capacitor (BV30) in Murata technology with minimal dielectric thickness)

Table 5 summarizes the lifetime predictions at different values of applied stress voltage (V_g) and temperatures, using the TDDB E-model at 0.1% cumulative failures, for PICSHV50 3D-capacitors (BV50) with minimal dielectric thickness:

Vg (V)	37°C	100°C	150°C	225°C
13	1392 years	347 years	155 years	62 years
17	278 years	69 years	30 years	12 years
21	55 years	13 years	6.1 years	2.4 years
25	11 years	2.7 years	1.2 years	181 days

Table 5: Lifetime predictions based on TDDB E-model
(PICSHV50 capacitor (BV50) in Murata technology with minimal dielectric thickness)

Table 6 summarizes the lifetime predictions at different values of applied stress voltage (V_g) and temperatures, using the TDDB E-model at 0.1% cumulative failures, for PICSHV100 (BV100) 3D-capacitors with minimal dielectric thickness:

Vg (V)	37°C	100°C	150°C	225°C
28	305 years	49 years	17 years	5.2 years
32	98 years	16 years	5.5 years	1.7 years
36	32 years	5.1 years	1.8 years	198 days
40	10 years	1.6 years	210 days	64 days

Table 6: Lifetime predictions based on TDDB E-model
(PICSHV100 (BV100) capacitor in Murata technology with minimal dielectric thickness)

Reliability predictions

Failure rate

Failure rate (λ) is defined as the number of products that failed between t and t+Δt. It is expressed in FITs (Failures In Time) which correspond to the number of failures that can be expected in one billion (10^9) device-hours of operation.

Figure 7 and Table 6 present one-year projected failure rates for PICS3 (BV11) capacitor, for various values of voltage and temperature conditions.

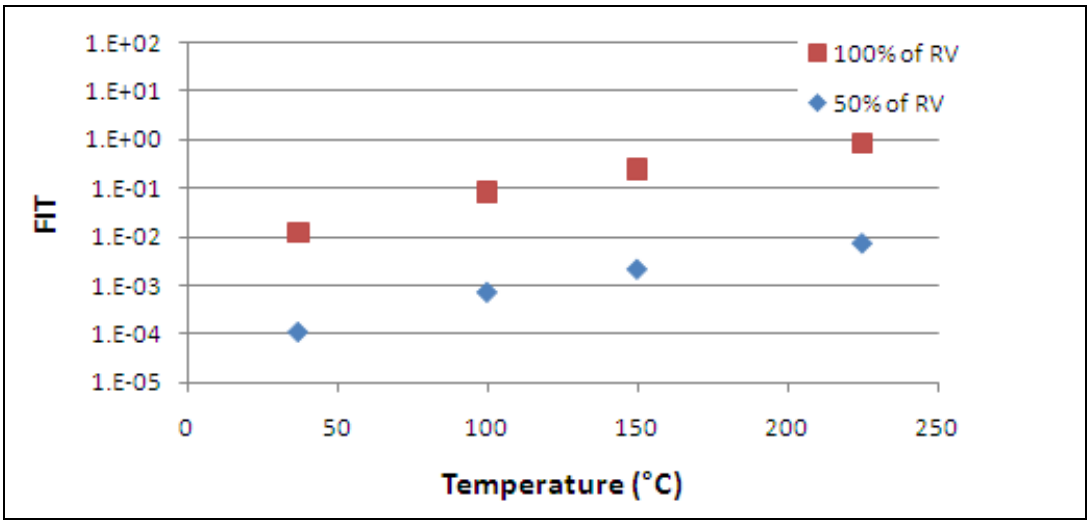

Figure 7: PICS3 (BV11) capacitors failure rate (1 FIT = 1 Failure in 109 hours)

Note: RV = Rated Voltage (maximum voltage that can be continuously applied to the capacitor)
RV = 3.3V for PICS3 (BV11) technology

Vg	37°C	100°C	150°C	225°C
50% of RV	0.0001	0.0007	0.0021	0.0073
100% of RV	0.0125	0.0831	0.250	0.863

Table 7: Failure In Time of PICS3 (BV11) capacitor (in FITs)

MTBF

Mean Time Between Failures (MTBF) is estimated by the total time on all systems divided by the number of failures. MTBF is derived from failure rate as described in Equation (3)

$$MTBF = 10^9/FITs \quad (3)$$

Calculations of MTBF for PICS3 (BV11) capacitor are listed in Table 8.

Vg	37°C	100°C	150°C	225°C
50% of RV	1.08E+09	1.63E+08	5.41E+07	1.57E+07
100% of RV	9.13E+06	1.37E+06	4.56E+05	1.32E+05

Table 8 : Calculations of Mean Time Between Failures for PICS3 (BV11) capacitor (in years)

MTTF

Median Time To Failure (MTTF or t_{50}) is defined to occur when 50% of the products have failed.

Calculations of MTTF for PICS3 (BV11) capacitor are listed in Table 9.

Vg	37°C	100°C	150°C	225°C
50% of RV	1.14E+06	3.21E+05	1.55E+05	6.86E+04
100% of RV	4.70E+04	1.32E+04	6.40E+03	2.83E+03

Table 9 : Calculations of Median Time to Failure for PICS3 (BV11) capacitor (in years)

Comparison with other capacitor technologies

Application scenarios

Table 10 depicts the three scenarios chosen to make reliability predictions. The application conditions used in the prediction model represent three potential use conditions in medical implantable and general medical electronic applications.

Application	Scenario	Voltage	Temperature
Medical Implantable	1	100% of RV	37°C
Medical implantable	2	50% of RV	37°C
Elevated temperature	3	50% of RV	85°C

Table 10: Application scenarios

Comparison with X7R and Ta capacitors

Given the varying scenarios, we can predict projected Failure In Time, projected failure rate and Median Time To Failure. Table 11 summarizes the PICS3 versus discrete competitors (ceramic X7R and Tantalum)

Technology	Scenario	Failure In Time (FIT)	Projected Failure Rate in 10 years (ppm)	Predicted Median Time To Failure (years)
X7R	1	1.31E-01	11.5	4.40E+04
	2	9.44E-03	0.8	6.20E+05
	3	2.14E+00	187	2.50E+03
Ta	1	6.30E+01	5526	9.05E+02
	2	5.04E-01	44	1.13E+05
	3	5.60E+00	491	1.02E+04
PICS3	1	1.25E-02	1	4.70E+04
	2	1.05E-04	0.5	1.14E+06
	3	4.74E-04	2	4.17E+05

Table 11 : Comparison of PICS3 capacitors with X7R and Ta capacitors

For the 3 scenarios, the projected failure rate in 10 years in PICS3 (BV11) is less than 1 ppm. Thanks to Murata technology on silicon, the typical failure rate is 10 times lower than standard SMD's.

In comparison with the Ta & X7R capacitors, the improvement provided by PICS3 (BV11) is emphasized when the temperature is increased.

Thermal cycling performances

Purpose

Temperature Cycling test (TMCL) is conducted for the purpose of determining the resistance of a part to exposure at extreme high and low temperatures. Effects of temperature cycling include cracking and delamination of finishes, cracking and crazing of embedding and encapsulation compounds, opening of thermal seals and case seams, leakage of filling materials, and changes in electrical characteristics due to mechanical displacement or rupture of conductors or of insulating materials.

Technology qualification vehicle

The Technology qualification vehicle is a 5.3mm * 5.3mm silicon die in Murata technology PICS3 (BV11), grinded at 100µm thickness, assembled in a HVQFN48 package, as illustrated in Figure 8.

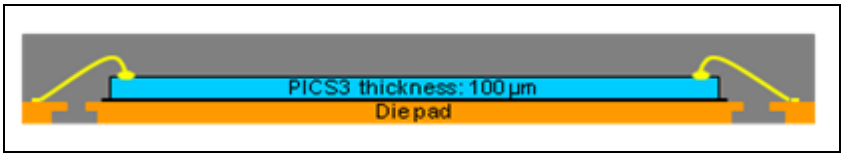

Figure 8: package used for process qualification

Test methodology

TMCL tests are done at package level on a minimum of 231 DUT (Device Under Test) from 3 lots with no more than 90 DUT from any one lot. Parts are preconditioned per JESD22-A113 and tested prior to temperature cycling. Technology qualification vehicle is exposed to 1000 cycles -65°C / +150°C (Jedec condition C), with intermediate test point at 200 cycles. Effect of Thermal Cycling is illustrated on Figure 9.

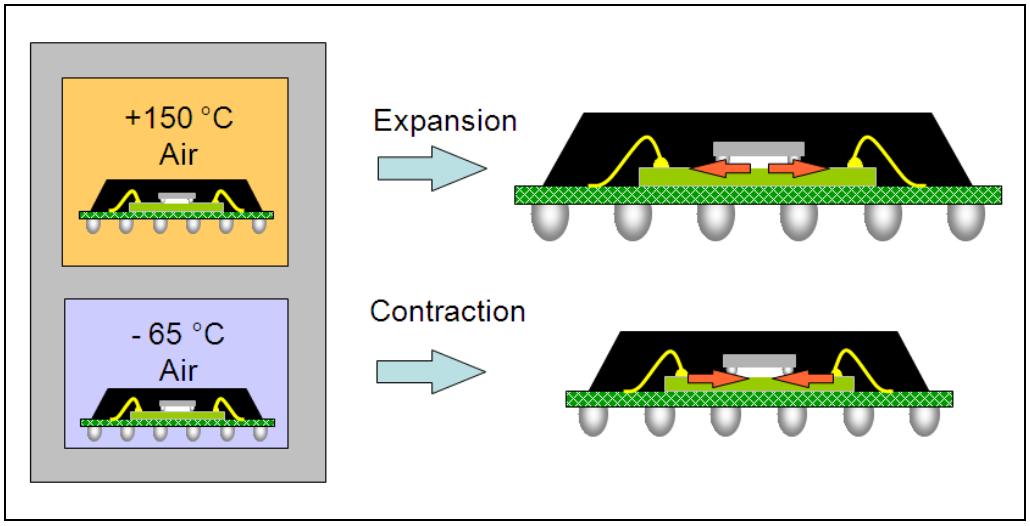

Figure 9: Effect of Thermal Cycling

Coffin-Manson model

Acceleration factor (AF) due to temperature cycling test is described by the Coffin-Manson Equation (4):

$$AF = (\Delta T_{stress}/\Delta T_{use})^n \quad (4)$$

with ΔT_{stress} = temperature swing during stress test

ΔT_{use} = temperature swing during use

n = Coffin Manson exponent; 3.0 for 3D Murata technologies

In Table 12, the typical use conditions for a number of common applications (High End Server, Avionic Cockpit, Telecom Hand Held Application…) have been compared to 3 possible test conditions: condition C (-65°C / +150°C), condition B (-55°C / +125°C) and condition G (-40°C / +125°C).

							Condition C (-65 / +150)			Condition B (-55 / +125)			Condition G (-40 / +125)		
Application	Operational Mode	Environmental & Power Cycles	Operational Temp Cycle Range (°C)	Delta use (°C)	Field Lifetime (years)	Cycles	AF	Equivalent cycles	Total cycles	AF	Equivalent cycles	Total cycles	AF	Equivalent cycles	Total cycles
Desk Top Computer with energy saving	Main	1/day	20 / 60	40	5.0	1826	155	12	15	91	20	25	70	26	33
	Mini	17/day	52 / 60	8		31046	19411	2		11391	3		8774	4	
	Short	1/day	40 / 60	20		1826	1242	1		729	3		562	3	
High End Server		4/year	14 / 55	41	11.0	44	144	0.3	0.3	85	0.5	0.5	65	0.7	0.7
Avionic Cockpit		2.5/day	0 / 50	50	23.0	21002	80	264	264	47	450	450	36	584	584
Telecom Hand Held Application	Talk	20/day	32 / 70	38	5.0	36525	181	202	202	106	344	344	82	446	446
	Standby / Off	1/day	30 / 32	2		1826	1242297	0		729000	0		561516	0	
Telecom Uncontrolled	Power	1/month		85	15.0	180	16	11	20	9	19	34	7	25	43.7
	Env	1/day	____	25		5479	636	9		373	15		287	19	
Telecom Controlled	Power	1/month		85	15.0	180	16	11.1	11.2	9	19	19.2	7	25	24.9
	Env	1/day		6		5479	46011	0.1		27000	0.2		20797	0	
Automotive Underhood (Grade 0)		5/day	-40 / 150	190	15.0	27394	1.4	18906	18906	0.9	32218	32218	0.7	41827	41827

Table 12: Equivalent cycles for common applications

In the case of Telecom Hand Held Application, 5.0 year field lifetime is equivalent to 202 cycles condition C, 344 cycles condition B or 446 cycles condition G.

In Table 13, the equivalent lifetime has been computed in function of the number of stress cycles.

Nc cycles stress (-65°C +150°C)	1000	500	200	100
Lifetime (years) - Desk Top Computer	337	169	67	34
Lifetime (years) - High End Server	36050	18025	7210	3605
Lifetime (years) - Avionic Electronics in Cockpit	87.1	43.5	17.4	8.7
Lifetime (years) - Telecom Hand Held	**24.8**	**12.4**	**5.0**	**2.5**
Lifetime (years) - Telecom Uncontrolled	1033	517	207	103
Lifetime (years) - Telecom Controlled	1343	671	269	134
Lifetime (years) - Automotive Underhood (grade 0)	0.8	0.4	0.2	0.1
Nc cycles stress (-55°C +125°C)	1000	500	200	100
Lifetime (years) - Desk Top Computer	198	99	40	20
Lifetime (years) - High End Server	21155	10577	4231	2115
Lifetime (years) - Avionic Electronics in Cockpit	51.1	25.5	10.2	5.1
Lifetime (years) - Telecom Hand Held	**14.5**	**7.3**	**2.9**	**1.5**
Lifetime (years) - Telecom Uncontrolled	606	303	121	61
Lifetime (years) - Telecom Controlled	788	394	158	79
Lifetime (years) - Automotive Underhood (grade 0)	0.5	0.2	0.1	0.0
Nc cycles stress (-40°C +125°C)	1000	500	200	100
Lifetime (years) - Desk Top Computer	152	76	30	15
Lifetime (years) - High End Server	16294	8147	3259	1629
Lifetime (years) - Avionic Electronics in Cockpit	39.4	19.7	7.9	3.9
Lifetime (years) - Telecom Hand Held	**11.2**	**5.6**	**2.2**	**1.1**
Lifetime (years) - Telecom Uncontrolled	467	233	93	47
Lifetime (years) - Telecom Controlled	607	303	121	61
Lifetime (years) - Automotive Underhood (grade 0)	0.4	0.2	0.1	0.0

Table 13: Equivalent lifetime vs. number of stress cycles

In the case of Telecom Hand Held Application, TMCL stress of 500 cycles condition C (-65°C / +150°C) is equivalent to 12.4 year lifetime.

Murata technology PICS3 (BV11) TMCL performances

TMCL results of Murata technology PICS3 (BV11) qualification vehicle, for cycles of -65°C / +150°C, were fitted to Weibull law illustrated by Figure 10.

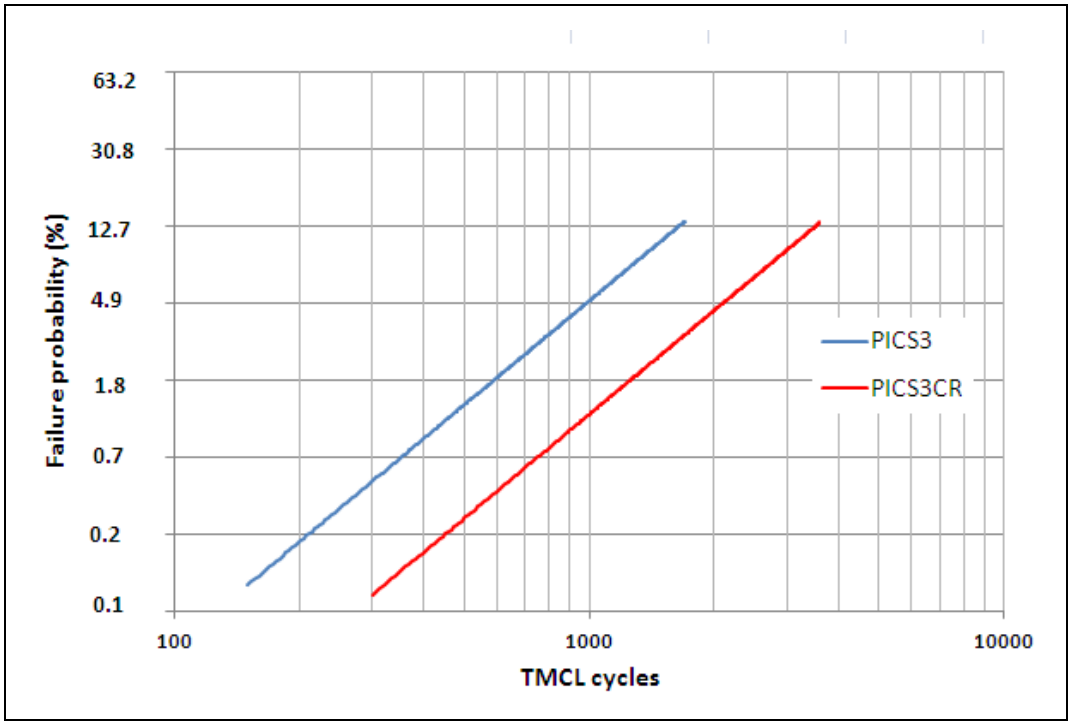

Figure 10: Weibull plot of TMCL tests on Murata technology PICS3/PICS3CR qualification vehicles

Extraction of Weibull distribution enables the calculation of the lifetime for common applications (High End Server, Avionic Cockpit, Telecom Hand Held Application…). Table 14 presents the expected lifetime for the Murata technology PICS3 qualification vehicle in function of the failure criteria.

Failure criteria	1%	0.1%	0.01%	0.001%
PPM	10000	1000	100	10
Lifetime (years) - Desk Top Computer	146	45	14	4
Lifetime (years) - High End Server	15628	4774	1461	447
Lifetime (years) - Avionic Electronics in Cockpit	37.7	11.5	3.5	1.1
Lifetime (years) - Telecom Hand Held	**10.7**	**3.3**	**1.0**	**0.3**
Lifetime (years) - Telecom Uncontrolled	448	137	42	13
Lifetime (years) - Telecom Controlled	582	178	54	17
Lifetime (years) - Automotive Underhood (grade 0)	0.3	0.1	0.0	0.0

Table 14: lifetime of Murata technology PICS3 (BV11) qualification vehicle vs. failure criteria

In the case of Telecom Hand Held Application, cumulative failure for Murata technology PICS3 (BV11) qualification vehicle is 1% after 10.7 years in use.

Murata technology PICS3CR TMCL performances

Murata developed a process option (PICS3CR) for increased TMCL performances. This process option is recommended in case of large silicon dice in high-constraint packages.

3 * 77 DUT were exposed to 500 cycles -65°C / +150°C (Jedec condition C), with intermediate test point at 200 cycles. No failure was observed up to 500 cycles.

This no-failure situation demonstrates that TMCL performances have been significantly improved. For the following analysis, the first failure is assumed to be imminent. As no failure has occurred, this is a conservative engineering assumption in order to evaluate the lower bounds of lifetime for Murata technology PICS3CR, presented in Table 15, for common applications (High End Server, Avionic Cockpit, Telecom Hand Held Application…).

Failure criteria	1%	0.1%	0.01%	0.001%
PPM	10000	1000	100	10
Lifetime (years) - Desk Top Computer	312	95	29	9
Lifetime (years) - High End Server	33386	10199	3122	956
Lifetime (years) - Avionic Electronics in Cockpit	80.6	24.6	7.5	2.3
Lifetime (years) - Telecom Hand Held	**23.0**	**7.0**	**2.1**	**0.7**
Lifetime (years) - Telecom Uncontrolled	957	292	89	27
Lifetime (years) - Telecom Controlled	1244	380	116	36
Lifetime (years) - Automotive Underhood (grade 0)	0.7	0.2	0.1	0.0

Table 15 : lower bounds of lifetime for Murata technology PICS3CR

In the case of Telecom Hand Held Application, cumulative failure for Murata technology PICS3CR is less than 1% after 23 years in use.

Simulation tools

- Cadence environment
- RF Simulator: Spectre and Momentum

Packaging

- Bare die
- WLCSP with bumps
- BGA, HVQFN… packages
- Support SiP assembly flow

Packing

- Tape and Reel
- Tray
- Foil

Revision history

Revision	Date	Description	Author
3.2	29/07/19	Layout update	Canelle G.
3.3	30/09/19	Add PICSHV100 data	Canelle G.
3.4	19/10/21	Add BV information to loop the link with Technical datasheets	Canelle G.

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www.murata.com
mis@murata.com