Datasheet

Type 2EA Wi-Fi® + Bluetooth® Module

Infineon CYW55573 Chipset for 802.11a/b/g/n/ac/ax 2x2 MIMO + Bluetooth 5.3 - Rev. F

- Sample P/N: LBEE5XV2EA-SMP

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About This Document

Type 2EA is a small and high-performance module based on IFX CYW55573 combo chipset, supporting IEEE 802.11a/b/g/n/ac/ax 2x2 MIMO + Bluetooth 5.3 BR/EDR/LE. This datasheet describes Type 2EA module in detail.

Please be aware that an important notice concerning availability, standard warranty and use in critical applications of Murata products and disclaimers thereto appears at the end of this specification sheet.

Audience & Purpose

Intended audience includes any customer looking to integrate this module into their product; specifically RF, hardware, software, and systems engineers.

Document Conventions

Table 1 describes the document conventions.

Table 1: Document Conventions

Conventions	Description
	Warning Note Indicates very important note. Users are strongly recommended to review.
	Info Note Intended for informational purposes. Users should review.
	Menu Reference Indicates menu navigation instructions. **Example**: Insert➔Tables➔Quick Tables➔Save Selection to Gallery
	External Hyperlink This symbol indicates a hyperlink to an external document or website. **Example**: Embedded Artists AB Click on the text to open the external link.
	Internal Hyperlink This symbol indicates a hyperlink within the document. **Example**: Scope Click on the text to open the link.
`Console input/output or code snippet`	**Console I/O or Code Snippet** This text ***Style*** denotes console input/output or a code snippet.
`# Console I/O comment` `// Code snippet comment`	**Console I/O or Code Snippet Comment** This text ***Style*** denotes a console input/output or code snippet comment. • Console I/O comment (preceded by "#") is for informational purposes only and does not denote actual console input/output. • Code Snippet comment (preceded by "//") may exist in the original code.

1 Scope

This specification characterizes the IEEE 802.11a/b/g/n/ac/ax 2x2 MIMO + Bluetooth 5.3 BR/EDR/LE combo module.

2 Key Feature

The salient features of Type 2EA are

- Infineon CYW55573 inside
- Supports IEEE 802.11a/b/g/n/ac/ax: Tri band 2.4 GHz, 5 GHz, and 6 GHz
- 2x2 MIMO with 20 MHz, 40 MHz and 80 MHz channels
- Supports Bluetooth specification version 5.3
- For supported Bluetooth functions, refer to Bluetooth SIG site ☐
- WLAN interface: PCIe 3.0 Gen2, SDIO 3.0/2.0
- Bluetooth interface: HCI UART
- Temperature Range: -40 °C to 85 °C
- Dimensions 12.5 x 9.4 x 1.2 mm
- Weight: 0.36 mg
- MSL: 3
- Surface-mount type
- RoHS compliant
- Total FIT: 286

3 Ordering Information

The ordering information are shown in **Table 2.**

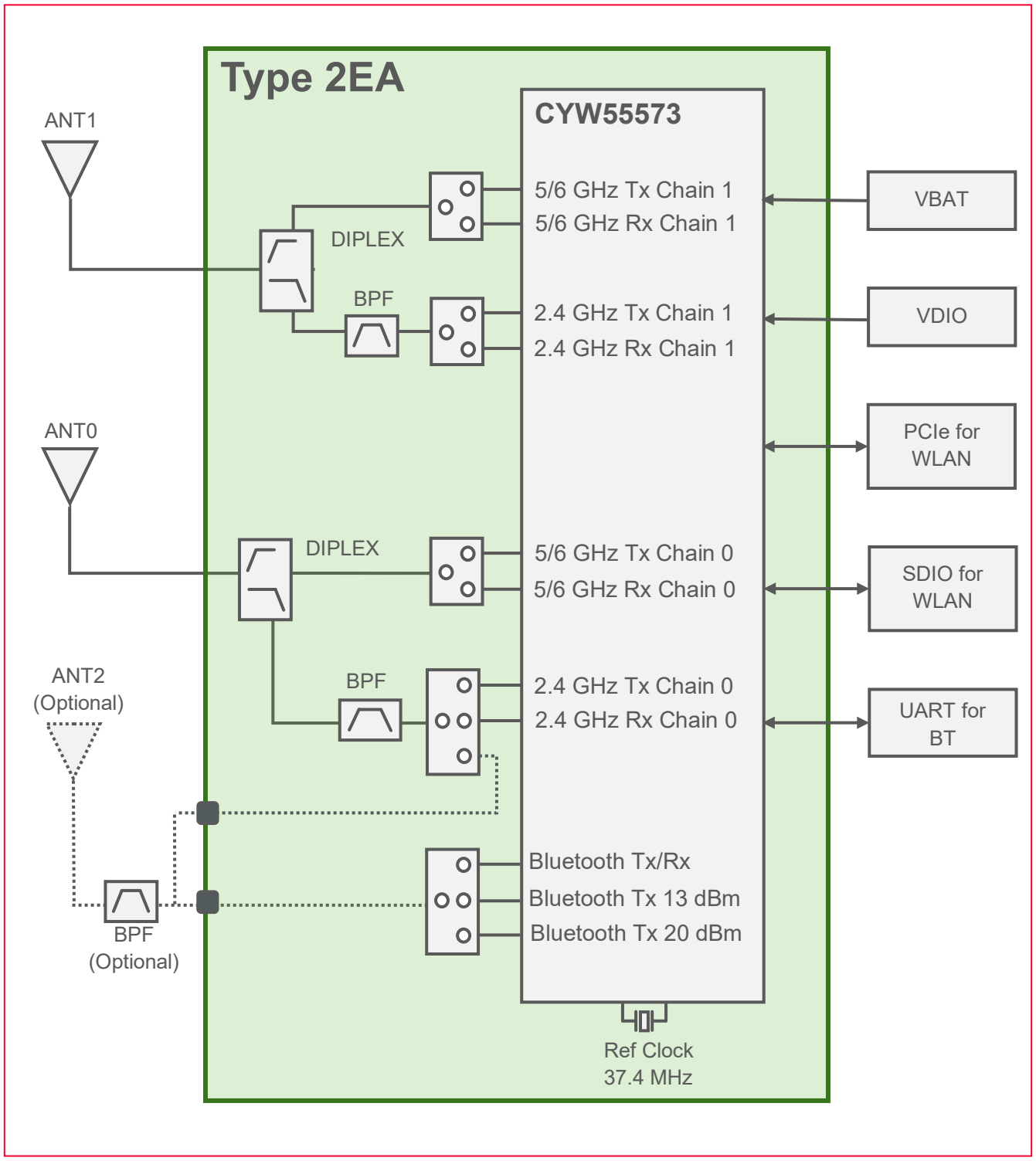
Table 2: Ordering Information

Ordering Part Number	Description
LBEE5XV2EA-802	Module Order
LBEE5XV2EA-SMP	Sample module order (If module samples are not available through distribution, contact Murata referencing this part number)
EAR00413	Embedded Artists Type 2EA M.2 EVB (default EVB available through distribution)
LBEE5XV2EA-EVB	Murata Type 2EA M.2 EVB (contact Murata as this is special order item)

4 Block Diagram

Figure 1 shows the block diagram.

Figure 1: Block Diagram



5 Dimensions, Marking, and Terminal Configurations

This section has information on dimensions, marking, and terminal configurations for Type 2EA as shown in **Figure 2**.

Figure 2: Dimension, Marking and Terminal Configuration (Unit: Millimeters)

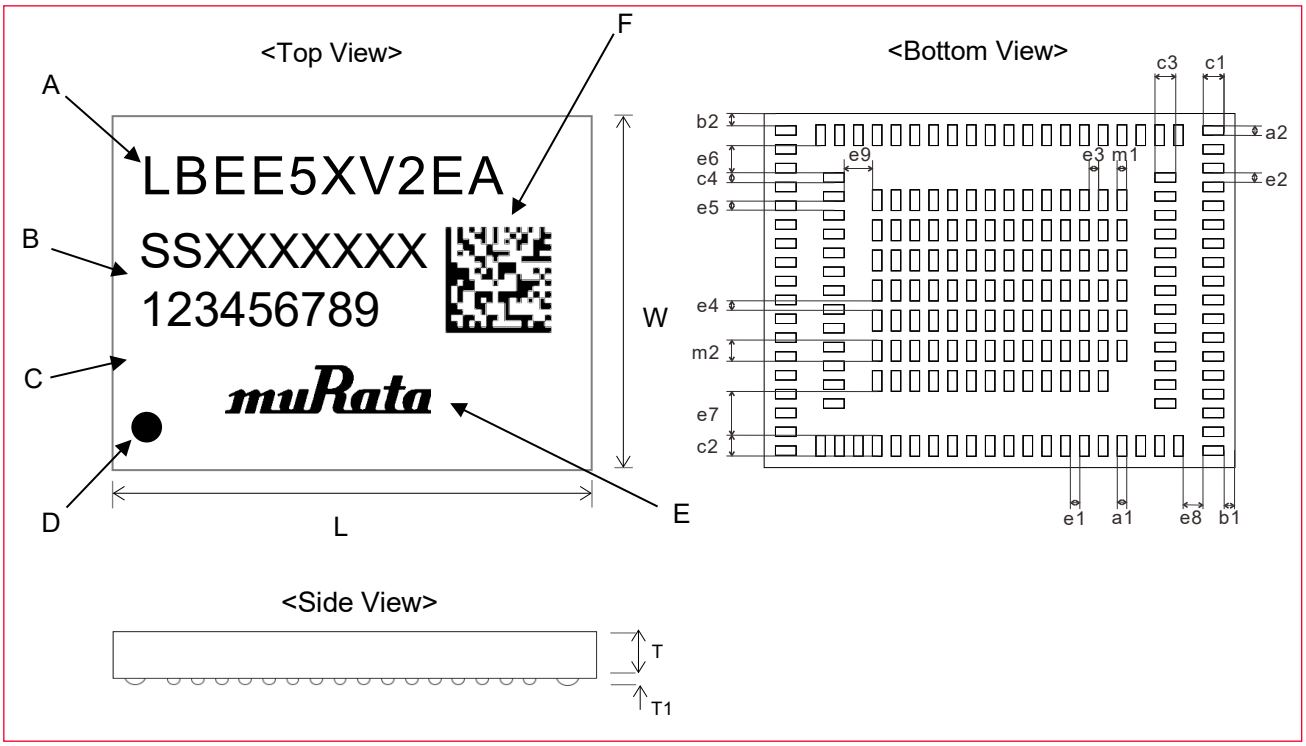


Table 3 describes the markings shown in **Figure 2**.

Table 3: Markings

Marking	Meaning
A	Module Part Number
B	Inspection Number
C	Serial Number
D	Pin 1 Marking
E	Murata Logo
F	2D code

Table 4: Dimensions (In Millimeters)

Mark	Dimensions	Mark	Dimensions	Mark	Dimensions	Mark	Dimensions
L	12.5 ± 0.2	W	9.4 ± 0.2	T	1.2 maximum	T1	0.04 typical
a1	0.25 ± 0.1	a2	0.25 ± 0.1	b1	0.30 ± 0.2	b2	0.30 ± 0.2
c1	0.55 ± 0.1	c2	0.55 ± 0.1	c3	0.55 ± 0.1	c4	0.25 ± 0.1
e1	0.25 ± 0.1	e2	0.25 ± 0.1	e3	0.25 ± 0.1	e4	0.25 ± 0.1
e5	0.25 ± 0.1	e6	0.725 ± 0.1	e7	1.175 ± 0.1	e8	0.525 ± 0.2
e9	0.75 ± 0.1	m1	0.25 ± 0.1	m2	0.55 ± 0.1		

6 Module Pin Descriptions

This section has the Pin descriptions of Type 2EA and pin assignments layout descriptions.

6.1 Module Pin Layout (Top View)

The pin assignment (Top View) layout is shown in **Figure 3**.

Figure 3: Pin Layout Top View

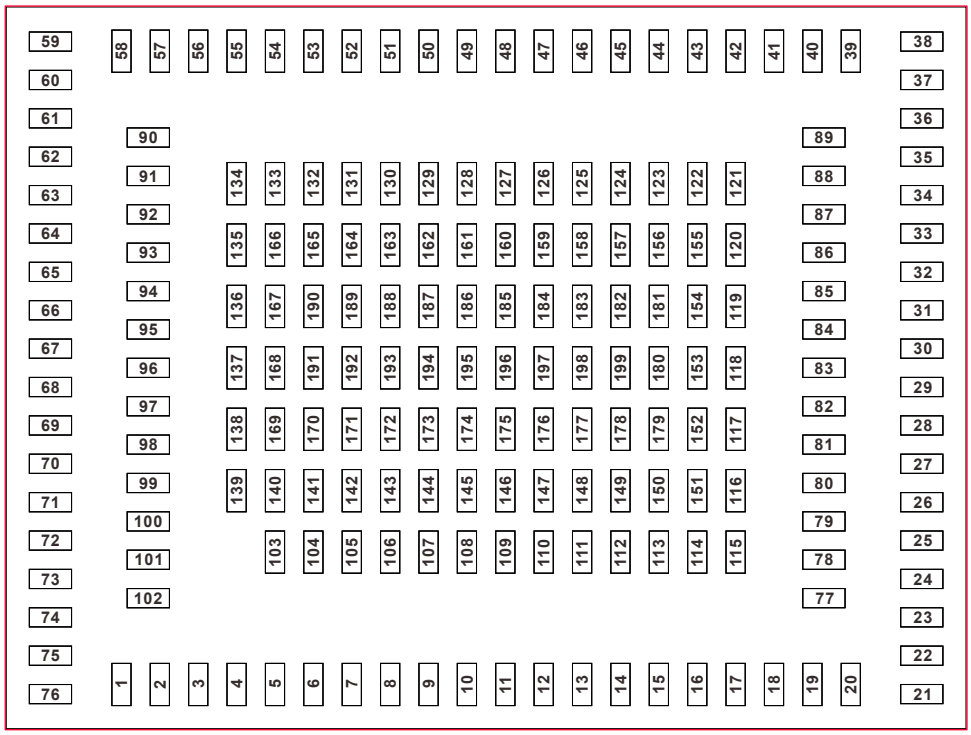


Table 5 illustrates the terminal configurations.

Table 5: Terminal Name Terminal Configurations

No.	Terminal Name	No.	Terminal Name	No.	Terminal Name
1	PCIE_PERST_L	37	ANT1	73	GND
2	PCIE_CLKREQ_L	38	GND	74	PCIE_REFCLKP
3	PCIE_PME_L	39	GND	75	PCIE_REFCLKN
4	GND	40	GPIO_8_WL_UART	76-95	GND
5	BT_PCM_SYNC	41	GPIO_1_WL_DEV_WAKE	96	MIC_P
6	BT_PCM_IN	42	GND	97	MIC_N
7	BT_PCM_CLK	43	GPIO_0_WL_HOST_WAKE	98	GND
8	BT_PCM_OUT	44	GPIO_7	99	BT_I2S_DO
9	GND	45	BT_REG_ON	100	BT_I2S_WS
10	I2S_DI	46	GND	101	BT_I2S_CLK
11	I2S_MCK	47	GND	102	BT_I2S_DI
12	I2S_SCK	48	GND	103	GND
13	I2S_LRCK	49	GND	104	GND
14	I2S_DO	50	GND	105	DMIC_DATA
15	GND	51	LPO_IN	106	DMIC_CLK

No.	Terminal Name	No.	Terminal Name	No.	Terminal Name
16	BT_UART_RXD	52	GND	107	GND
17	BT_UART_RTS_N	53	VDDOUT_RF3P3	108	GND
18	BT_UART_TXD	54	GND	109	BT_GPIO_2
19	BT_UART_CTS_N	55	VDDIO	110	BT_GPIO_9
20	GND	56	GND	111	GND
21	GND	57	VBAT_1	112	GND
22	BT_OUT	58	VBAT_2	113	GND
23	GND	59	GND	114	BT_GPIO_11
24	BT_IN	60	WL_REG_ON	115-124	GND
25	GND	61	SDIO_DATA_2	125	LHL_GPIO2
26	BT_DEV_WAKE	62	SDIO_DATA_0	126	LHL_GPIO3
27	BT_HOST_WAKE	63	SDIO_DATA_1	127	LHL_GPIO0
28	BT_CLK_REQ	64	SDIO_CMD	128	RF_SW_CTRL16
29	GND	65	SDIO_CLK	129	RF_SW_CTRL14
30	ANT0	66	SDIO_DATA_3	130	RF_SW_CTRL15
31	GND	67	GND	131	GPIO_12
32	LHL_GPIO1	68	PCIE_RDP	132	GND
33	GPIO_10_WL_UART	69	PCIE_RDN	133	GND
34	GPIO_11_WL_UART	70	GND	134	N.C
35	GPIO_9_WL_UART	71	PCIE_TDP	135-199	GND
36	GND	72	PCIE_TDN		

6.2 Pin Descriptions

Table 6 describes Type 2EA Pins.

Table 6: Pin Descriptions

No.	Pin name	Type	Connection to IC Pin Name	Description
1	PCIE_PERST_L	I	PCIE_PERST_L	PCIe System Reset. This input is the PCIe reset as defined in the PCIe base specification v1.1.
2	PCIE_CLKREQ_L	OD	PCIE_CLKREQ_L	PCIe clock request signal which indicates when the REFCLK to the PCIe interface can be gated. • **1** = the clock can be gated. • **0** = the clock is required.
3	PCIE_PME_L	OD	PCI_PME_L	PCI power management event output. Used to request a change in the device or system power state. The assertion and de-assertion of this signal is asynchronous to the PCIe reference clock. This signal has an open-drain output structure, as per the PCI Bus Local Bus Specification, revision 2.3.
4	GND			Ground
5	BT_PCM_SYNC		BT_GPIO_18	Bluetooth General Purpose I/O
6	BT_PCM_IN		BT_GPIO_17	Bluetooth General Purpose I/O
7	BT_PCM_CLK		BT_GPIO_19	Bluetooth General Purpose I/O
8	BT_PCM_OUT		BT_GPIO_16	Bluetooth General Purpose I/O

No.	Pin name	Type	Connection to IC Pin Name	Description
9	GND			Ground
10	I2S_DI	I/O	I2S_DI	I2S Serial Data Input
11	I2S_MCK	I/O	I2S_MCK	I2S Master Clock
12	I2S_SCK	I/O	I2S_SCK	I2S Bit or Serial Clock
13	I2S_LRCK	I/O	I2S_LRCK	I2S Word Clock or Left/Right Clock
14	I2S_DO	I/O	I2S_DO	I2S Serial Data Output
15	GND			Ground
16	BT_UART_RXD	I	BT_UART_RXD	UART serial input. Serial data input for the HCI UART interface.
17	BT_UART_RTS_N	O	BT_UART_RTS_N	UART request-to-send. Active-low request-to-send signal for the HCI UART interface. BT LED control pin.
18	BT_UART_TXD	O	BT_UART_TXD	UART Serial Output. Serial data output for the HCI UART interface.
19	BT_UART_CTS_N	I	BT_UART_CTS_N	UART clear-to-send. Active-low clear-to-send signal for the HCI UART interface.
20	GND			Ground
21	GND			Ground
22	BT_OUT	RF		RF Port for Bluetooth.
23	GND			Ground
24	BT_IN	RF		RF port for WLAN/Bluetooth shared antenna.
25	GND			Ground
26	BT_DEV_WAKE	I/O	BT_DEV_WAKE	Bluetooth DEVICE WAKE
27	BT_HOST_WAKE	I/O	BT_HOST_WAKE	Bluetooth HOST WAKE
28	BT_CLK_REQ		BT_GPIO_20	Bluetooth wants the host to turn on the reference clock. BT_CLK_REQ polarity is active-high.
29	GND			Ground
30	ANT0	RF		RF Port for WLAN (2.4 GHz, 5 GHz, and 6 GHz) and BT.
31	GND			Ground
32	LHL_GPIO1	I/O	LHL_GPIO1	Miscellaneous General Purpose I/O
33	GPIO_10_WL_UART	I/O	GPIO_10	WLAN General Purpose I/O
34	GPIO_11_WL_UART	I/O	GPIO_11	WLAN General Purpose I/O
35	GPIO_9_WL_UART		GPIO_9	WLAN General Purpose I/O
36	GND			Ground
37	ANT1	RF		RF Port for WLAN (2.4 GHz, 5 GHz, and 6 GHz)
38	GND			Ground
39	GND			Ground
40	GPIO_8_WL_UART		GPIO_8	WLAN General Purpose I/O
41	GPIO_1_WL_DEV_WAKE		GPIO_1	WLAN DEVICE WAKE
42	GND			Ground
43	GPIO_0_WL_HOST_WAKE		GPIO_0	WLAN HOST WAKE
44	GPIO_7		GPIO_7	WLAN General Purpose I/O
45	BT_REG_ON	I	BT_REG_ON	Used by the PMU to power up or power down the internal CYW5557x regulators used by the BT section. When de-asserted, this pin holds the BT section in reset. This pin has an internal 50 kΩ pull-down resistor that is auto enabled/disabled by programming.

No.	Pin name	Type	Connection to IC Pin Name	Description
46-50	GND			Ground
51	LPO_IN	I	LPO_IN	External Sleep Clock Input (32.768 kHz)
52	GND			Ground
53	VDDOUT_RF3P3	PWR	VDDOUT_RF3P3 VDDIO_RFSW WRF_SYNTH_VDD_V3P3 WRF_PMU_VDD_V3P3_C0 WRF_PMU_VDD_V3P3_C1 Power supply for RF Switches	3.3 V Output to Supply WLAN Radio, RF Switchs, PMU
54	GND			Ground
55	VDDIO	PWR	VDDIO VDDIO_SD PMU_VDD1P8P PMU_VDD1P8A FLL_VDDIO WRF_VDD_V1P8_C0 WRF_VDD_V1P8_C1 BT_VDDO BT_VDDO_SMIF LHL_VDDO	1.8 V IO Supply for WLAN/Bluetooth GPIOs
56	GND			Ground
57	VBAT_1	PWR	CSR_VDDBAT ASR_VDDBAT BTLDO_VDDBAT WLLDO_VDDBAT	Battery Supply Input for CSR Power Stage, ASR Power Stage, BT PA LDO, and WLAN PA/RF LDO.
58	VBAT_2	PWR		
59	GND			Ground
60	WL_REG_ON	I	WL_REG_ON	Used by the PMU to power up or power down the internal CYW5557x regulators used by the WLAN section. When de-asserted, this pin holds the WLAN section in reset. This pin has an internal 50 KΩ pull-down resistor that is auto enabled/disabled by programming.
61	SDIO_DATA_2	I/O	SDIO_DATA_2	SDIO Data Line 2
62	SDIO_DATA_0	I/O	SDIO_DATA_0	SDIO Data Line 0
63	SDIO_DATA_1	I/O	SDIO_DATA_1	SDIO Data Line 1
64	SDIO_CMD	I/O	SDIO_CMD	SDIO Command Line
65	SDIO_CLK	I	SDIO_CLK	SDIO Clock Input
66	SDIO_DATA_3	I/O	SDIO_DATA_3	SDIO Data Line 3
67	GND			Ground
68	PCIE_RDP	I	PCIE_RDP	PCIE Receiver Differential Pair Positive Input
69	PCIE_RDN	I	PCIE_RDN	PCIE Receiver Differential Pair Negative Input
70	GND			Ground
71	PCIE_TDP	O	PCIE_TDP	PCIE Transmitter Differential Pair Positive Output
72	PCIE_TDN	O	PCIE_TDN	PCIE Transmitter Differential Pair Negative Output
73	GND			Ground
74	PCIE_REFCLKP	I	PCIE_REFCLKP	PCIE Differential Pair Clock Source (100 MHz) Positive Input.

No.	Pin name	Type	Connection to IC Pin Name	Description
75	PCIE_REFCLKN	I	PCIE_REFCLKN	PCIE Differential Pair Clock Source (100 MHz) Negative Input.
76-95	GND			Ground
96	MIC_P	I	MIC_P	ADC Microphone Positive Input
97	MIC_N		MIC_N	ADC Microphone Negative Input
98	GND			Ground
99	BT_I2S_DO	I/O	BT_GPIO_12	BT General Purpose I/O
100	BT_I2S_WS	I/O	BT_GPIO_14	BT General Purpose I/O
101	BT_I2S_CLK	I/O	BT_GPIO_15	BT General Purpose I/O
102	BT_I2S_DI	I/O	BT_GPIO_13	BT General Purpose I/O
103	GND			Ground
104	GND			Ground
105	DMIC_DATA	I/O	DMIC_DQ	Digital Mic Data
106	DMIC_CLK	I/O	DMIC_CK	Digital Mic Clock
107	GND			Ground
108	GND			Ground
109	BT_GPIO_2	I/O	BT_GPIO_2	BT General Purpose I/O
110	BT_GPIO_9	I/O	BT_GPIO_9	BT General Purpose I/O
111	GND			Ground
112	GND			Ground
113	GND			Ground
114	BT_GPIO_11	I/O	BT_GPIO_11	BT General Purpose I/O
115-124	GND			Ground
125	LHL_GPIO2	I/O	LHL_GPIO2	Miscellaneous General Purpose I/O
126	LHL_GPIO3	I/O	LHL_GPIO3	Miscellaneous General Purpose I/O
127	LHL_GPIO0	I/O	LHL_GPIO0	Miscellaneous General Purpose I/O
128	RF_SW_CTRL16	O	RF_SW_CTRL16	Programmable RF switch control lines. The control lines are programmable via the driver and NVRAM file.
129	RF_SW_CTRL14	O	RF_SW_CTRL14	Programmable RF switch control lines. The control lines are programmable via the driver and NVRAM file.
130	RF_SW_CTRL15	O	RF_SW_CTRL15	Programmable RF switch control lines. The control lines are programmable via the driver and NVRAM file.
131	GPIO_12	I/O	GPIO_12	WLAN General Purpose I/O
132	GND			Ground
133	GND			Ground
134	N.C			No Connection
135-199	GND			Ground

7 Absolute Maximum Ratings

The absolute and maximum ratings are shown in **Table 7.**

Table 7: Absolute Maximum Ratings

Parameter		Minimum	Maximum	Unit
Storage Temperature		-40	+85	^{0}C
Supply Voltage	VBAT	-0.5	6.0	V
	VDDIO	-0.5	2.2	V

Stresses in excess of the absolute ratings may cause permanent damage. Functional operation is not implied under these conditions. Exposure to absolute ratings for extended periods of time may adversely affect reliability. No damage assuming only one parameter is set at limit at a time with all other parameters is set within operating condition.

8 Operating Condition

The operating conditions are shown in **Table 8**.

Table 8: Operating Conditions

Parameter		Minimum	Typical	Maximum	Unit
Operating Temperature		-40	25	85	°C
Specification Temperature		-30	25	70	°C
Operating Voltage	VBAT	3.0	3.3	4.8	V
	VDDIO	1.71	1.8	1.89	V
Peak Current	VBAT=3.3V	-	-	1000	mA

Minimum voltage of VBAT is sensitive to get RF performance, so please keep minimum. Voltages level at the input of these module terminals, otherwise RF performance significantly goes worse.

9 External LPO_IN Signal Requirement

External LPO requirements are shown in **Table 9**.

Table 9: External LPO_IN Signal Requirement

Parameter	External LPO_IN Clock	Unit
Nominal input frequency	32.768	kHz
Frequency accuracy	±250	ppm
Duty cycle	30 - 70	%
Input signal amplitude	200–3300	mV, p-p
Signal type	Square-wave or sinewave	
Input impedance[2]	> 100k	Ω
	< 5	pF
Clock jitter (during initial start-up)	< 10,000	ppm

10 Strapping Options

The pins listed in Table below are sampled at power-on reset (POR) to determine the various operating modes. Sampling occurs a few milliseconds after an internal POR or de-assertion of the external POR. After the POR, each pin assumes the GPIO, or alternative function specified in the signal descriptions table. Each strapping option pin has an internal pull-up (PU) or pull-down (PD) resistor that determines the default mode. To change the mode, connect an external PU resistor to VDDIO or a PD resistor to GND, using a 10 kΩ resistor or less.

Table 10 shows the strapping options.

Table 10: Strapping Options

Pin Name	Default Pull During Strapping	
GPIO_1	1	• **1** = PCIE • **0** = SDIO
GPIO_12	1	• **1** = Bluetooth over UART • **0** = Reserved

[2] When power is applied or switch off.

11 I/O State

The following notations are used in I/O State Table.

- **I**: Input signal
- **O**: Output signal
- **I/O**: Input/Output signal
- **PU** = Pulled up
- **PD** = Pulled down
- **NoPull** = Neither pulled up nor pulled down

Where applicable, the default value is shown in brackets (for example, [default value]).

Table 11 describes the I/O state table.

Table 11: I/O State Table

Name	I/O	Keeper	Active Mode	Low-Power State/Sleep (All Power Present)	Power-down (BT_REG_ON and WL_REG_ON Held Low)	Out-of-Reset: Before SW Download (BT_REG_ON High; WL_REG_ON High)	(WL_REG_ON High and BT_REG_ON = 0) and VDDIOs are Present	Power Rail
WL_REG_ON BT_REG_ON	I	N	I: PD Pull-down auto disabled	I: PD Pull-down auto disabled	I: PD (of 50K)	I: PD (of 50K)	I: PD (of 50K)	
GPIO_0_WL_HOST_WAKE	I/O	Y	I/O: PU, PD, NoPull Programmable [PD]	I/O: PU, PD, NoPull Programmable [PD]	High-Z, NoPull	High-Z, NoPull	High-Z, NoPull	VDDIO
GPIO_1_WL_DEV_WAKE	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	High-Z, NoPull	High-Z, NoPull	VDDIO
GPIO_7	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I:NoPull	I:NoPull	VDDIO
GPIO_8_WL_UART	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I:NoPull	I:NoPull	VDDIO
GPIO_9_WL_UART	I/O	Y	I/O: PU, PD, NoPull Programmable [PU]	I/O: PU, PD, NoPull Programmable [PU]	High-Z, NoPull	I:NoPull	I:NoPull	VDDIO
GPIO_10_WL_UART	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I:NoPull	I:NoPull	VDDIO
GPIO_11_WL_UART	I/O	Y	I/O: PU, PD, NoPull Programmable [PU]	I/O: PU, PD, NoPull Programmable [PU]	High-Z, NoPull	I:NoPull	I:NoPull	VDDIO
GPIO_12	I/O	N	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	High-Z, NoPull	High-Z, NoPull	VDDIO

Name	I/O	Keeper	Active Mode	Low-Power State/Sleep (All Power Present)	Power-down (BT_REG_ON and WL_REG_ON Held Low)	Out-of-Reset: Before SW Download (BT_REG_ON High; WL_REG_ON High)	(WL_REG_ON High and BT_REG_ON = 0) and VDDIOs are Present	Power Rail
RF_SW_CTRL_X	O	N	O: NoPull	O: NoPull	High-Z, NoPull	O: NoPull	O: NoPull	VDDOUT_RF3P3
I2S_LRCK	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PD	I: PD	VDDIO
I2S_SCK	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PD	I: PD	VDDIO
I2S_MCK	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PD	I: PD	VDDIO
I2S_DI	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PD	I: PD	VDDIO
I2S_DO	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PD	I: PD	VDDIO
BT_GPIO_2	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PD	I: PD	VDDIO
BT_GPIO_9	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PD	I: PD	VDDIO
BT_GPIO_11	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PD	I: PD	VDDIO
BT_I2S_DO BT_GPIO_12	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PD	I: PD	VDDIO
BT_I2S_DI BT_GPIO_13	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PD	I: PD	VDDIO
BT_I2S_WS BT_GPIO_14	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PD	I: PD	VDDIO
BT_I2S_CLK BT_GPIO_15	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PD	I: PD	VDDIO
BT_PCM_OUT BT_GPIO_16	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PD	I: PD	VDDIO
BT_PCM_IN BT_GPIO_17	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PD	I: PD	VDDIO
BT_PCM_SYNC	I/O	Y	I/O: PU, PD, NoPull	I/O: PU, PD, NoPull	High-Z, No Pull	I: PD	I: PD	VDDIO

Name	I/O	Keeper	Active Mode	Low-Power State/Sleep (All Power Present)	Power-down (BT_REG_ON and WL_REG_ON Held Low)	Out-of-Reset: Before SW Download (BT_REG_ON High; WL_REG_ON High)	(WL_REG_ON High and BT_REG_ON = 0) and VDDIOs are Present	Power Rail
BT_GPIO_18			Programmable [NoPull]	Programmable [NoPull]				
BT_PCM_CLK BT_GPIO_19	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PD	I: PD	VDDIO
BT_CLK_REQ BT_GPIO_20	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	I: PD	O: No Pull	O: No Pull	VDDIO
BT_DEV_WAKE	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PD	I: PD	VDDIO
BT_HOST_WAKE	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PD	I: PD	VDDIO
LHL_GPIO0	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: No Pull	I: No Pull	VDDIO
LHL_GPIO1	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: No Pull	I: No Pull	VDDIO
LHL_GPIO2	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: No Pull	I: No Pull	VDDIO
LHL_GPIO3	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: No Pull	I: No Pull	VDDIO

12 Power-On Sequence

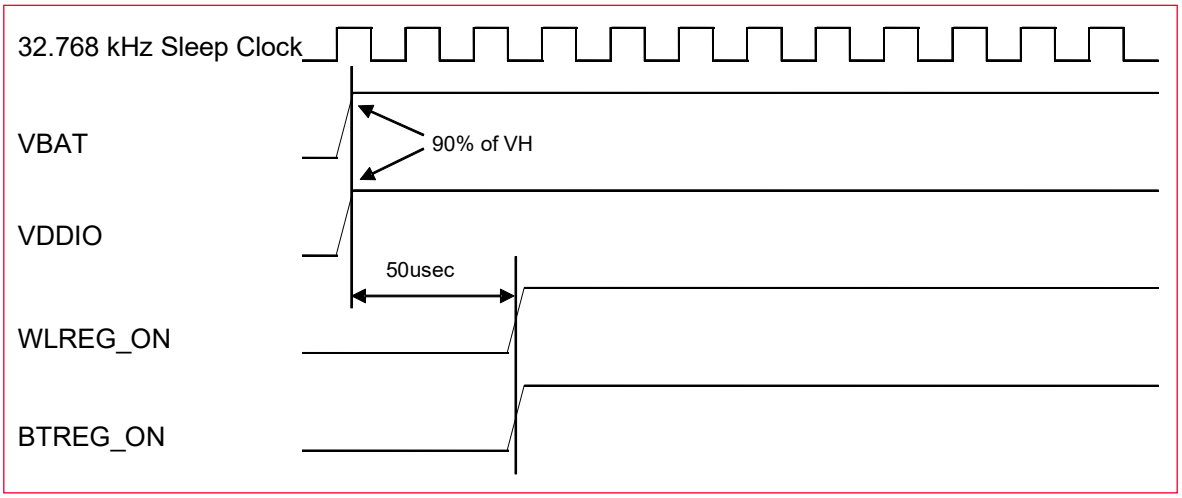
This section describes the power sequences along with their parameters.

- VBAT and VDDIO should not rise 10%-90% faster than 40 microseconds.
- VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present fast or be held high before VBAT is high.
- WLREG_ON and BTREG_ON should be up after sleep clock oscillation is stabilized.
- Please proceed reset by WLREG_ON and BTREG_ON until it starts normally if it doesn't wake from sleep property, or it is presented with uncertain status.
- CYW55573 has an internal power-on reset (POR) circuit. The device will be held in reset for a maximum of 110 ms after internal regulators and VDDIO have both passed the POR threshold. Wait at least 150 ms after internal regulators and VDDIO are available before initiating PCIe accesses.

12.1 Power-On Sequence for WLAN = ON and BT = ON

Figure 4 shows the power-on sequence diagram for WLAN = ON and BT = ON.

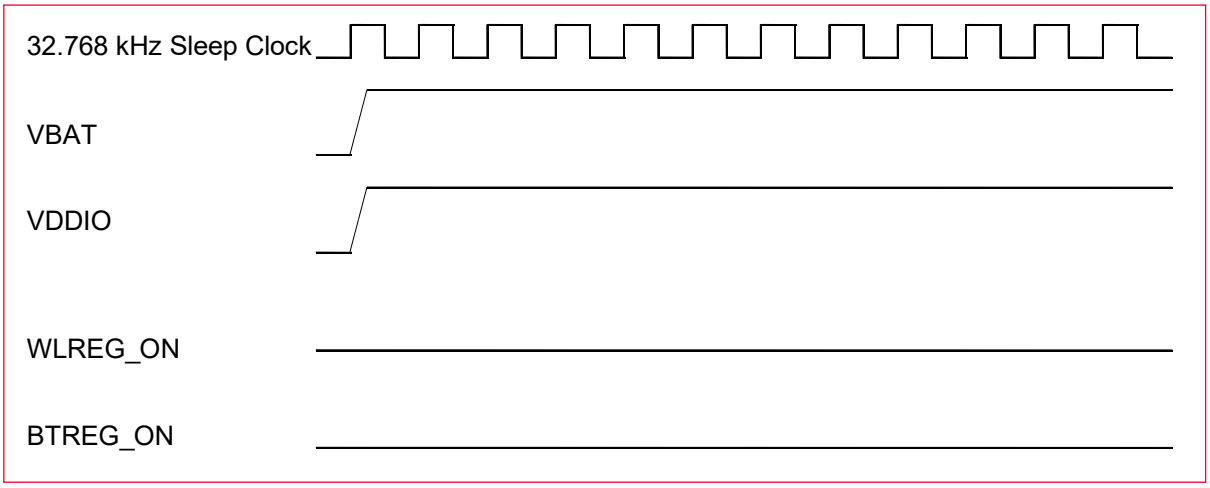
Figure 4: Power-On Sequence for WLAN = ON and BT = ON



12.2 Power-On Sequence for WLAN = OFF and BT = OFF

Figure 5 shows the power-on sequence diagram for WLAN = OFF and BT = OFF.

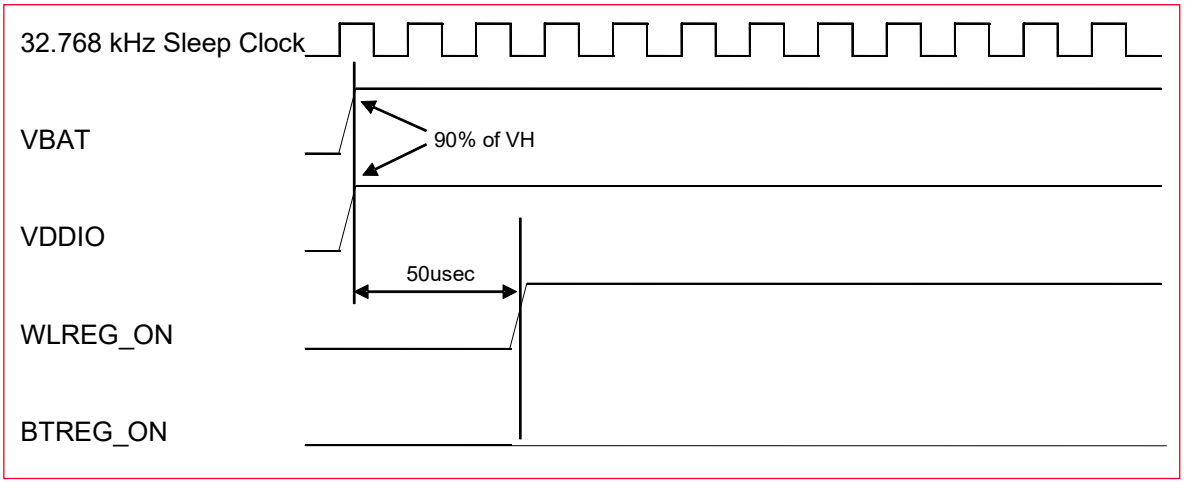
Figure 5: Power-On Sequence for WLAN = OFF and BT = OFF



12.3 Power-On Sequence for WLAN = ON and BT = OFF

Figure 6 shows the power-on sequence diagram for WLAN = ON and BT = OFF.

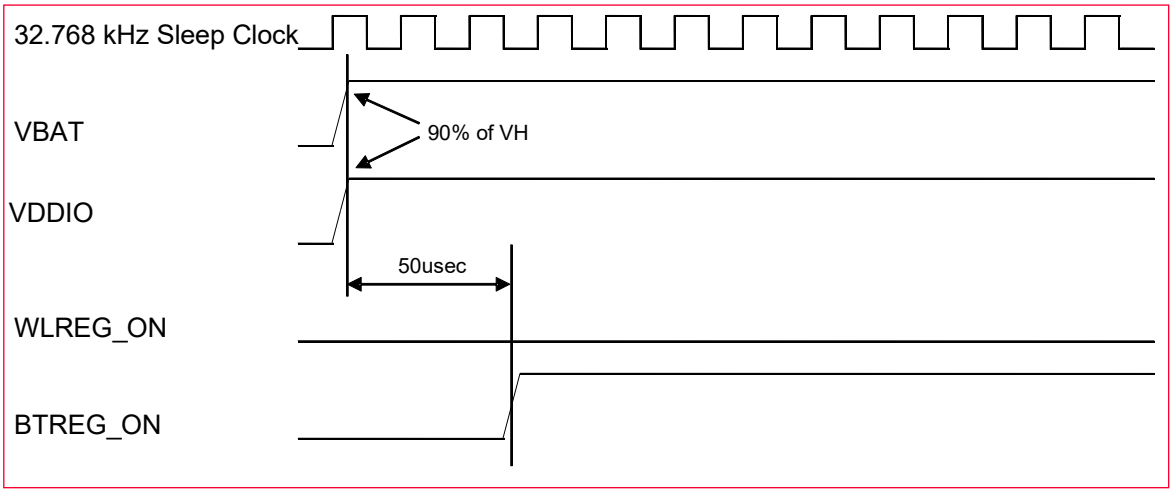
Figure 6: Power-On Sequence for WLAN = ON and BT = OFF



12.4 Power-On Sequence for WLAN = OFF and BT = ON

Figure 7 shows the power-on sequence diagram for WLAN = OFF and BT = ON.

Figure 7: Power-On Sequence for WLAN = OFF and BT = ON



13 Interface Timing and AC Characteristics

This section describes the Bluetooth UART timing and Bluetooth PCM interface timing data formatting and wideband speech support (at different modes) and their parameters.

13.1 Bluetooth UART Timing

Figure 8 shows the Bluetooth UART timing signals.

Figure 8: Bluetooth UART Timing

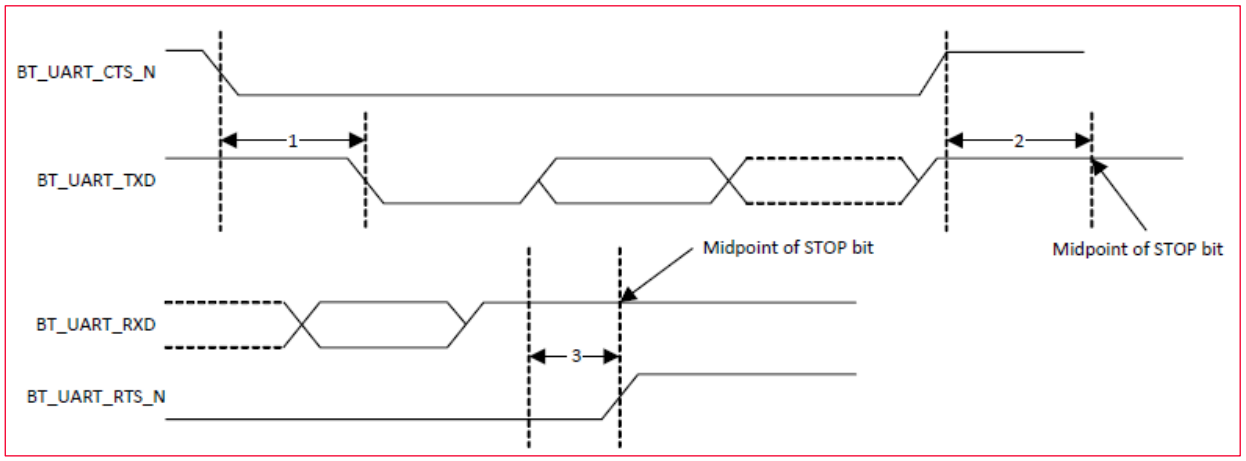


Table 12 shows the Bluetooth UART Timing Parameters.

Table 12: Bluetooth UART Timing Parameters

Reference	Description	Minimum	Typical	Maximum	Unit
1	Delay time, BT_UART_CTS_N low to BT_UART_TXD valid.			1.5	Bit periods
2	Setup time, BT_UART_CTS_N high before midpoint of stop bit.			0.5	Bit periods
3	Delay time, midpoint of stop bit to BT_UART_RTS_N high.			0.5	Bit periods

13.2 Bluetooth PCM Interface Timing

This section describes the Bluetooth PCM Interface Timing and its data formatting and widespread speed support that includes short frame sync and long frame sync at master and slave modes.

13.2.1 Data Formatting

The IC used in the module may be configured to generate and accept several different data formats. For conventional narrowband speech mode, the IC uses 13 of the 16 bits in each PCM frame. The location and order of these 13 bits can be configured to support various data formats on PCM interface. The remaining three bits are ignored on the input and may be filled with 0s, 1s, a sigh bit, or a programmed value on the output. The default format is 13bit 2's complement data, left justified, and clocked MSB first.

13.2.2 Wideband Speech Support

When the host encodes wideband speech (WBS) packets in transparent mode, the encoded packets are transferred over the PCM bus for an eSCO voice connection. In this mode, the PCM bus is typically configured in master mode for a 4 KHz sync rate with 16-bit samples, resulting in a 64-kbps bit rate. The IC also supports slave transparent mode using a proprietary rate-matching scheme. IN SBC-code mode, linear 16-bit data at 16 KHz (256 kbps rate) is transferred over the PCM bus.

13.2.3 Short Frame Sync, Master Mode

Figure 9 shows the short sync, slave mode signals.

Figure 9: Short Frame Sync, Master Mode

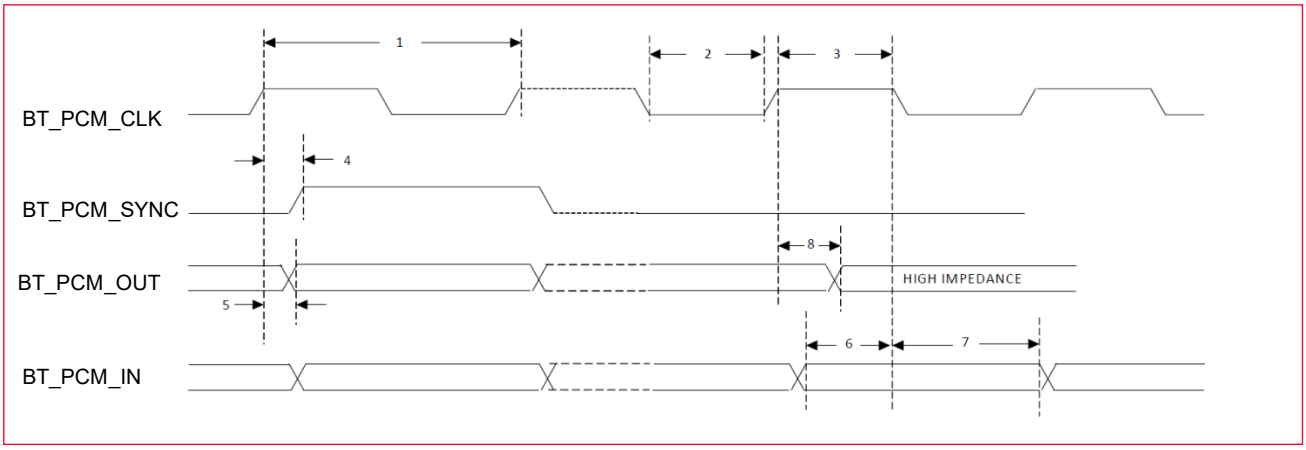


Table 13 describes the short frame sync, master mode parameters.

Table 13: Short Frame Sync, Master Mode Parameters

Reference	Description	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency			12.0	MHz
2	PCM bit clock High	41.0			ns
3	PCM bit clock Low	41.0			ns
4	PCM_SYNC delay	0		25.0	ns
5	PCM_OUT delay	0		25.0	ns
6	PCM_IN setup	8			ns
7	PCM_IN hold	8			ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance.	0		25.0	ns

13.2.4 Short Frame Sync, Slave Mode

Figure 10 shows the short sync, slave mode signals.

Figure 10: Short Frame Sync, Slave Mode

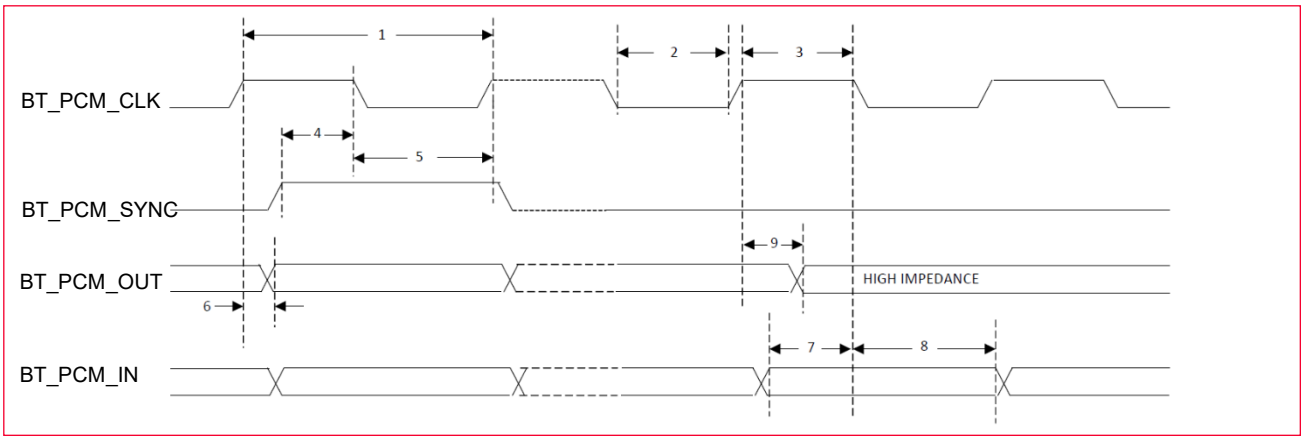


Table 14 describes the short frame sync, slave mode parameters.

Table 14: Short Frame Sync, Slave Mode Parameters

Reference	Description	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency			12.0	MHz
2	PCM bit clock High	41.0			ns
3	PCM bit clock Low	41.0			ns
4	PCM_SYNC setup	8.0			ns
5	PCM_SYNC hold	8.0			ns
6	PCM_OUT delay	0		25.0	ns
7	PCM_IN setup	8.0			ns
8	PCM_IN hold	8.0			ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance.	0	-	25.0	ns

13.2.5 Long Frame Sync, Master Mode

Figure 11 shows the long frame sync, master mode signals.

Figure 11: Long Frame Sync, Master Mode

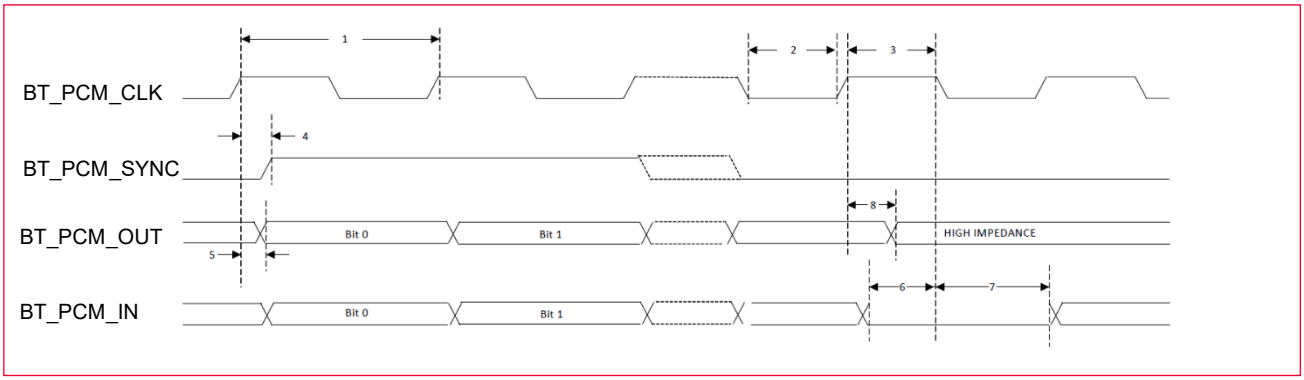


Table 15 describes the long frame sync, master mode parameters.

Table 15: Long Frame Sync, Master Mode Parameters

Reference	Description	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency			12.0	MHz
2	PCM bit clock High	41.0			ns
3	PCM bit clock Low	41.0			ns
4	PCM_SYNC delay	0		25.0	ns
5	PCM_OUT delay	0		25.0	ns
6	PCM_IN setup	8.0			ns
7	PCM_IN hold	8.0			ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0		25.0	ns

13.2.6 Long Frame Sync, Slave Mode

Figure 12 shows the long frame sync, slave mode signals.

Figure 12: Long Frame Sync, Slave Mode

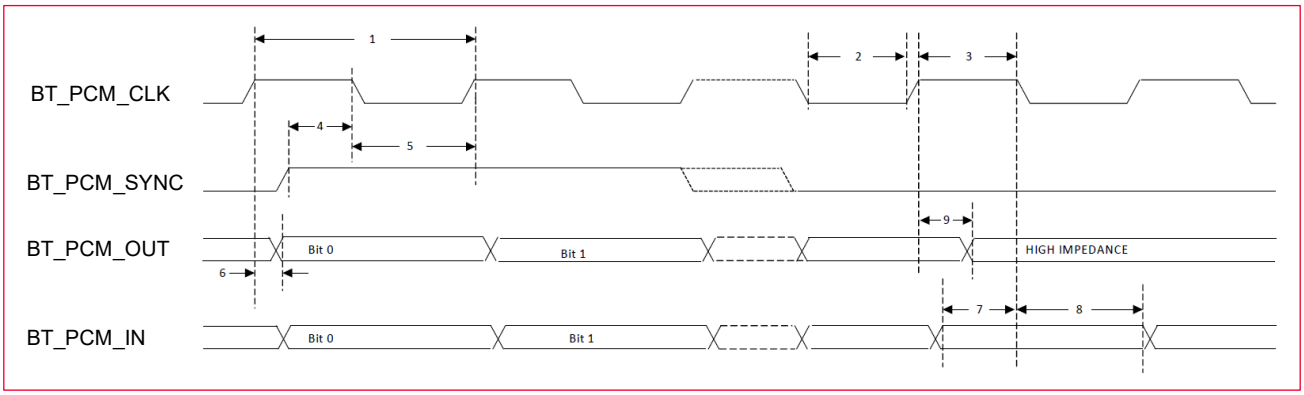


Table 16 describes the long frame sync, slave mode parameters.

Table 16: Long Frame Sync, Slave Mode Parameters

Reference	Description	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency			12.0	MHz
2	PCM bit clock High	41.0			Ns
3	PCM bit clock Low	41.0			Ns
4	PCM_SYNC setup	8.0			Ns
5	PCM_SYNC hold	8.0			Ns
6	PCM_OUT delay	0		25.0	Ns
7	PCM_IN setup	8.0			Ns
8	PCM_IN hold	8.0			ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance.	0		25.0	ns

13.3 Bluetooth I²S Interface Timing

The IC used in the module supports I²S format.

The I²S signals are:

- I²S clock: BT_I2S_CLK
- I²S Word Select: BT_I2S_WS
- I²S Data Out: BT_I2S_DO
- I²S Data In: BT_I2S_DI

BT_I2S_CLK and BT_I2S_WS become outputs in Master mode and inputs in Slave mode, whereas BT_I2S_DO always stays as an output. The channel word length is 16 bits, and the data is justified so that the MSB of the left-channel data is aligned with the MSB of the I_2S bus, in accord with the I2S specification. The MSB of each data word is transmitted one bit clock cycle after the BT_I2S_WS transition, synchronous with the falling edge of the bit clock. Left-channel data is transmitted when BT_I2S_WS is LOW, and right channel data is transmitted when BT_I2S_WS is HIGH. Data bits sent by CYW5557x are synchronized with the falling edge of BT_ I2S_CLK and should be sampled by the receiver on the rising edge of BT_I2S_CLK.

Table 17 describes the timing for I2S transmitters and receivers.

Table 17: Timing for I²S Transmitters and Receivers

	Transmitter				Receiver				Notes
	Lower Limit		Upper Limit		Lower Limit		Upper Limit		
	Minimum	Maximum	Minimum	Maximum	Minimum	Maximum	Minimum	Maximum	
Clock Period T	T_{tr}				T_r				a
Master Mode: Clock generated by transmitter or receiver									
HIGH t_{HC}	$0.35T_{tr}$				$0.35T_{tr}$				b
LOW t_{LC}	$0.35T_{tr}$				$0.35T_{tr}$				b
Slave Mode: Clock accepted by transmitter or receiver									
HIGH t_{HC}		$0.35T_{tr}$				$0.35T_{tr}$			c
LOW t_{LC}		$0.35T_{tr}$				$0.35T_{tr}$			c
Rise Time t_{RC}			$0.15T_{tr}$						d
Transmitter									
Delay t_{dtr}				0.8T					e
Hold time t_{htr}	0								d
Receiver									
Setup time t_{sr}					$0.2T_r$				f
Hold time t_{hr}					$0.2T_r$				f

The notes column is described below:

a) The system clock period T must be greater than T_{tr} and T_r because both the transmitter and receiver have to be able to handle the data transfer rate.

b) At all data rates in master mode, the transmitter or receiver generates a clock signal with a fixed mark/space ratio. For this reason, t_{HC} and t_{LC} specified with respect to T.

c) In slave mode, the transmitter and receiver need a clock signal with minimum HIGH and LOW periods so that they can detect the signal. So long as the minimum periods are greater than $0.35T_{tr}$ any clock that meets the requirements can be used.

d) Because the delay(t_{dtr}) and the maximum transmitter speed (defined by T_{tr}) are related, a fast transmitter driven by a slow clock edge can result in t_{dtr} not exceeding t_{RC} which means t_{htr} becomes zero or negative. Therefore, the transmitter has guarantee that t_{htr} is

greater than or equal to zero, so long as the clock rise-time t_{RC} is not more than t_{RC} where t_{RCmax} is not less than $0.15T_{tr}$.

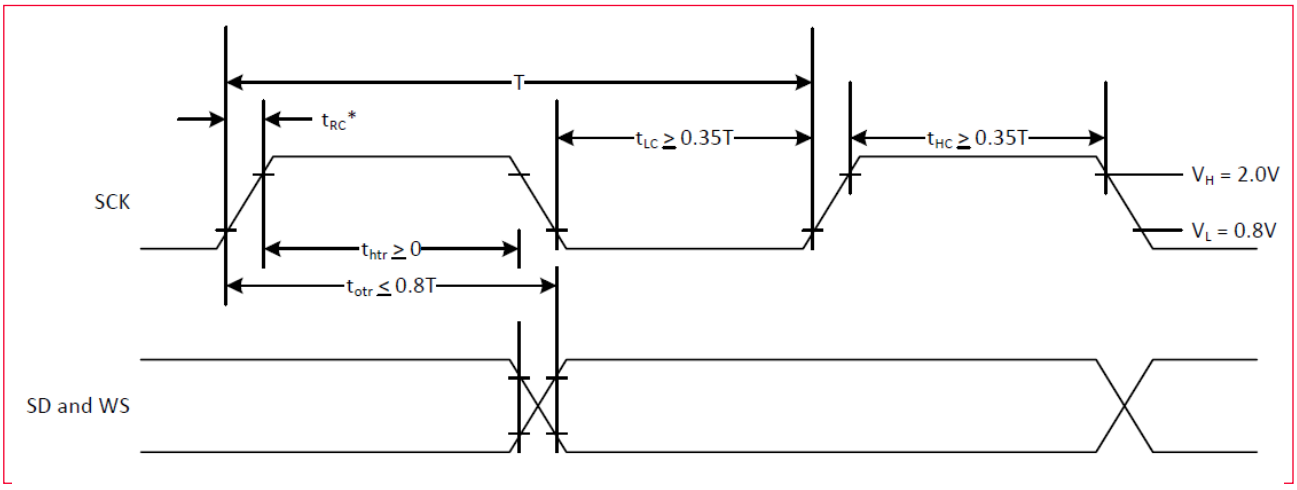
e) To allow data to be clocked out on a falling edge, the delay is specified with respect to the rising edge of the clock signal and T, always giving the receiver sufficient setup time.

f) The data setup and hold time must not be less than the specified receiver setup and hold time.

The time periods specified in below figures are defined by the transmitter speed. The receiver specifications must match transmitter performance.

Figure 13 shows the I²S transmitter timing signals.

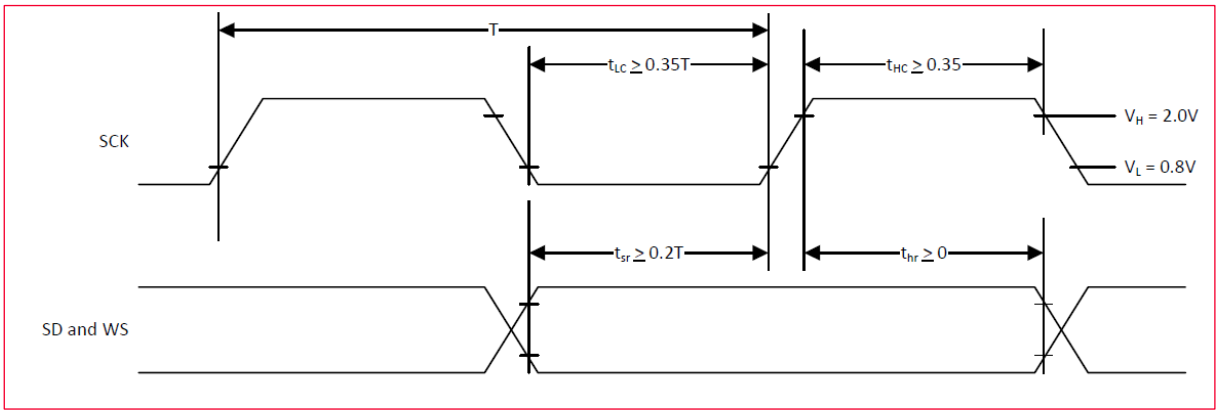
Figure 13: I²S Transmitter Timing



T = Clock period
T_{tr} = Minimum allowed clock period for transmitter
$T = T_{tr}$
t_{RC} is only relevant for transmitters in slave mode

Figure 14 shows the I²S receivers timing signals.

Figure 14: I²S Receivers Timing



T = Clock period
T_r = Minimum allowed clock period for transmitter
$T > T_r$

13.4 WLAN SDIO Timing

13.4.1 SDIO Default Mode Timing

Figure 15 and **Table 18** shows the SDIO default mode timing and its parameters.

Figure 15: SDIO Default Mode Timing

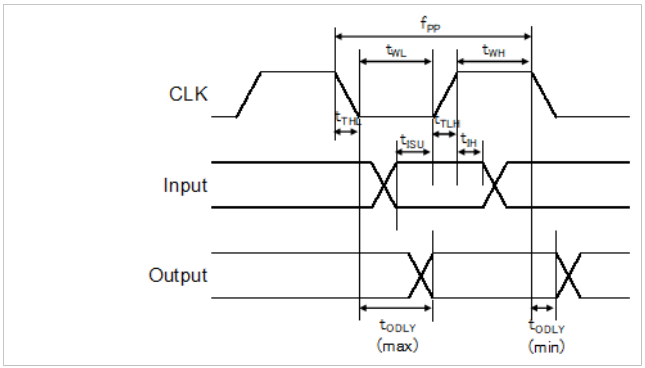


Table 18: SDIO Bus Timing[a] parameters (default Mode)

Parameter	Symbol	Min	Typ	Max	Unit
SDIO CLK (All values are referred to minimum VIH and maximum VIL[b]					
Frequency-Data Transfer Mode	fPP	0	-	25	MHz
Frequency-Identification Mode	fOD	0	-	400	kHz
Clock Low Time	tWL	10	-	-	ns
Clock High Time	tWH	10	-	-	ns
Clock Rise Time	tTLH	-	-	10	ns
Clock low Time	tTHL	-	-	10	ns
Inputs: CMD, DAT (referenced to CLK)					
Input Setup Time	tISU	5	-	-	ns
Input Hold Time	tIH	5	-	-	ns
Outputs: CMD, DAT (referenced to CLK)					
Output Delay time-Data Transfer Mode	tODLY	0	-	14	ns
Output Delay time-Identification Mode	tODLY	0	-	50	ns

(a). Timing is based on CL ≤ 40pF load on CMD and Data.
(b). Min (Vih) = 0.7*VIO and max (Vil) = 0.2*VIO.

13.4.2 SDIO High-Speed (HS) Mode Timing

Figure 16 and **Table 19** shows SDIO high speed mode timing and its parameters.

Figure 16: SDIO High-Speed Mode Timing

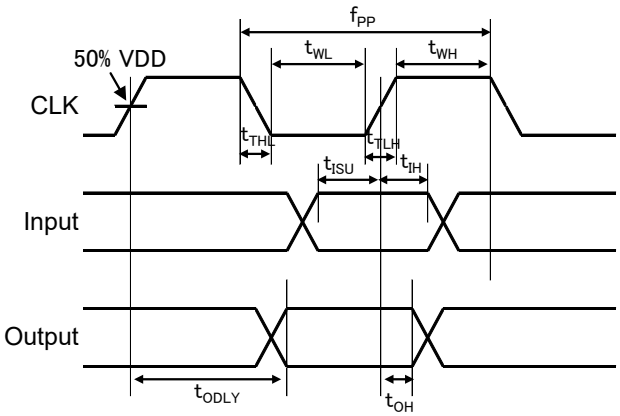


Table 19: SDIO Bus Timing[a] parameters (High-Speed Mode)

Parameter	Symbol	Min	Typ	Max	Unit
SDIO CLK (All values are referred to minimum VIH and maximum VIL[b]					
Frequency-Data Transfer Mode	fPP	0	-	50	MHz
Frequency-Identification Mode	fOD	0	-	400	kHz
Clock Low Time	tWL	7	-	-	ns
Clock High Time	tWH	7	-	-	ns
Clock Rise Time	tTLH	-	-	3	ns
Clock low Time	tTHL	-	-	3	ns
Inputs: CMD, DAT (referenced to CLK)					
Input Setup Time	tISU	6	-	-	ns
Input Hold Time	tIH	2	-	-	ns
Outputs: CMD, DAT (referenced to CLK)					
Output Delay time-Data Transfer Mode	tODLY	-	-	14	ns
Output Hold time	tOH	2.5	-	-	ns
Total System Capacitance (each line)	CL	-	-	40	pF

(a). Timing is based on CL ≤ 40pF load on CMD and Data.
(b). Min (Vih) = 0.7*VIO and max (Vil) = 0.2*VIO

13.4.3 SDIO Bus Timing Specifications in SDR Modes

Clock Timing

Figure 17 and **Table 20** shows SDIO bus clock timing and its parameters on SDR modes.

Figure 17: SDIO Clock Timing (SDR Modes)

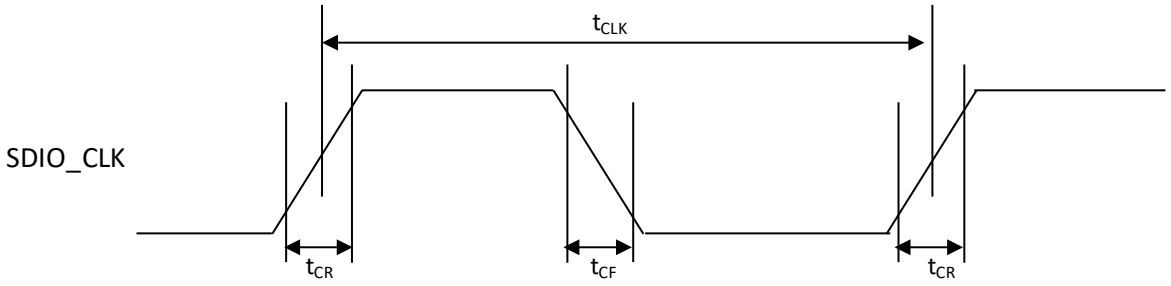


Table 20: SDIO Bus Clock Timing Parameters (SDR Modes)

Parameter	Symbol	Min	Max	Unit	Comments
-	tCLK	40	-	ns	SDR12 mode
		20	-	ns	SDR25 mode
		10	-	ns	SDR50 mode
		4.8	-	ns	SDR104 mode
-	tCR,tCF	-	0.2 x tCLK	ns	tCR,tCF<2.00ns(max)@100MHz,cCARD=10pF
					tCR,tCF<0.96ns(max)@208MHz,cCARD=10pF
Clock duty	-	30	70	%	-

Device Input Timing

Figure 18 and **Table 21** shows SDIO Bus input timing chart and its parameters on SDR modes.

Figure 18: SDIO Bus Input Timing (SDR Modes)

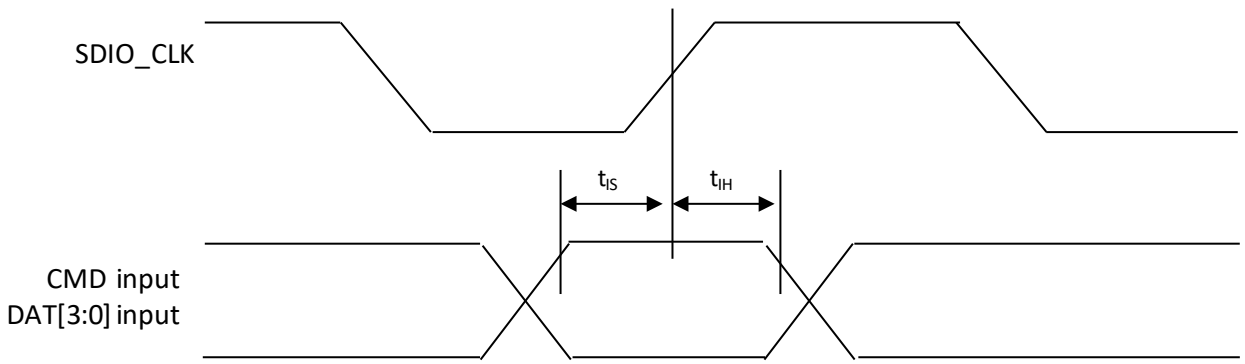


Table 21: SDIO Bus Input Timing Parameters (SDR Modes)

Symbol	Min	Max	Unit	Comments
SDR104 Mode				
tIS	1.4	-	ns	cCARD = 10pF,VCT = 0.975V
tIH	0.8	-	ns	cCARD = 5pF,VCT = 0.975V
SDR50 Mode				
tIS	3.0	-	ns	cCARD = 10pF,VCT = 0.975V
tIH	0.8	-	ns	cCARD = 5pF,VCT = 0.975V

Device Output Timing

Figure 19 and **Table 22** shows SDIO bus output timing and its parameters on SDR modes up to 100MHz.

Figure 19: SDIO Bus Ouput Timing (SDR Modes up to 100MHz)

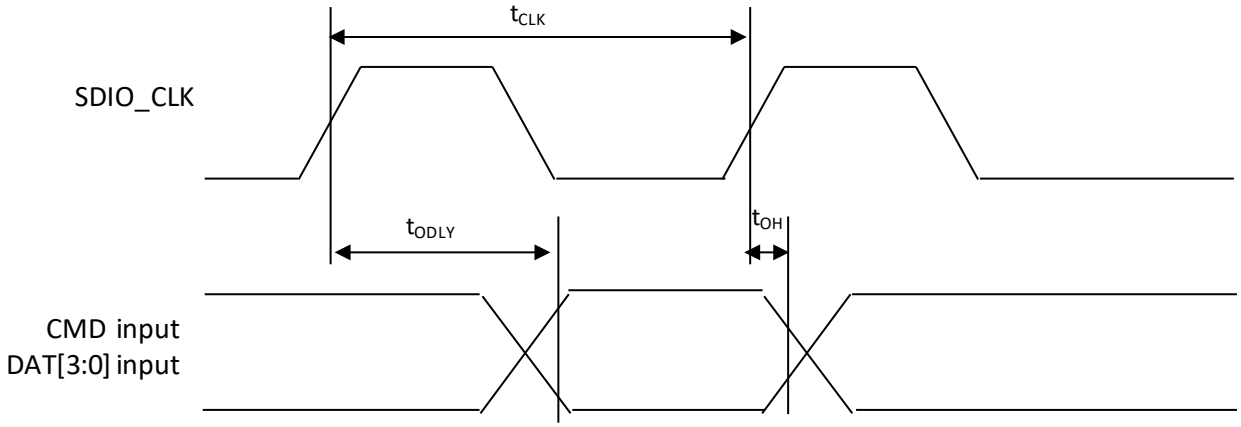


Table 22: SDIO Bus Ouput Timing Parameters (SDR Modes up to 100MHz)

Symbol	Min	Max	Unit	Comments
tODLY	-	7.5	ns	tCLK ≧ 10ns CL = 30pF using driver type B for SDR50
tODLY	-	14.0	ns	tCLK ≧ 20ns CL = 40pF using for SDR12,SDR25
tOH	1.5	-	ns	Hold time at the tODLY(min) CL = 15pF

Figure 20 and **Table 23** shows SDIO bus output timing its parameters on SDR modes 100MHz to 208MHz.

Figure 20: SDIO Bus Output Timing (SDR Modes 100MHz to 208MHz)

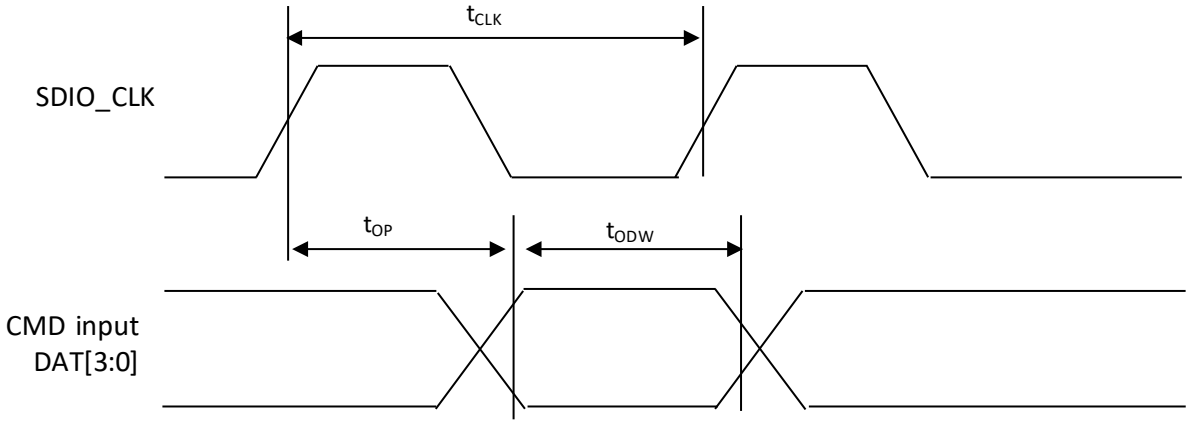


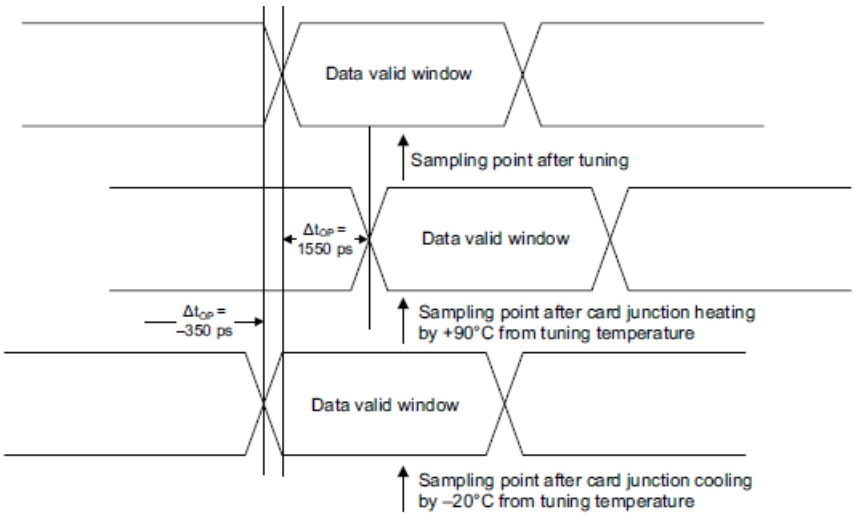
Table 23: SDIO Bus Ouput Timing Parameters (SDR Modes 100MHz to 208MHz)

Symbol	Min	Max	Unit	Comments
tOP	0	2	UI	Card output phase
Δ tOP	-350	+1550	ps	Delay variation due to temp change after tuning
tODW	0.60	-	UI	tODW = 2.88ns @208MHz

・Δtop=+1550ps for junction temperature of Δtop=90℃ during operation.
・Δtop=-350ps for junction temperature of Δtop=-20℃ during operation.
・Δtop=+2600ps for junction temperature of Δtop=-20℃ to +125℃ during operation

Figure 21 shows Δtop Consideration for Variable Data Window (SDR 104 Mode).

Figure 21: Δtop Consideration for Variable Data Window (SDR 104 Mode)



13.4.4 SDIO Bus Timing Specifications in DDR50 Mode

Figure 22 and **Table 24** shows SDIO Clock Timing and its parameters on DDR50 Mode.

Figure 22: SDIO Clock Timing (DDR50 Mode)

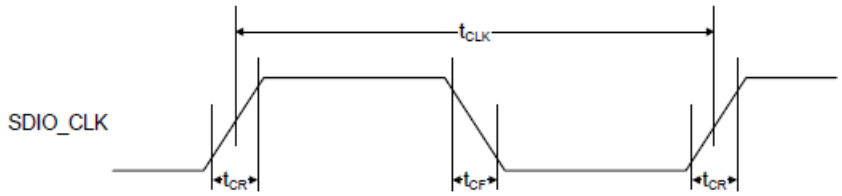


Table 24: SDIO Clock Timing Parameters (DDR50 Mode)

Parameter	Symbol	Min	Max	Unit	Comments
-	tCLK	20	-	ns	DDr50 mode
-	tCR, tCF	-	0.2 x tCLK	ns	tCR, tCF<4.00ns(max)@50MHz, cCard=10pF
Clock duty cycle	-	45	55	%	-

Figure 23 and **Table 25** shows SDIO Data Timing and its parameters on DDR50 Mode.

Figure 23: SDIO Data Timing (DDR50 Mode)

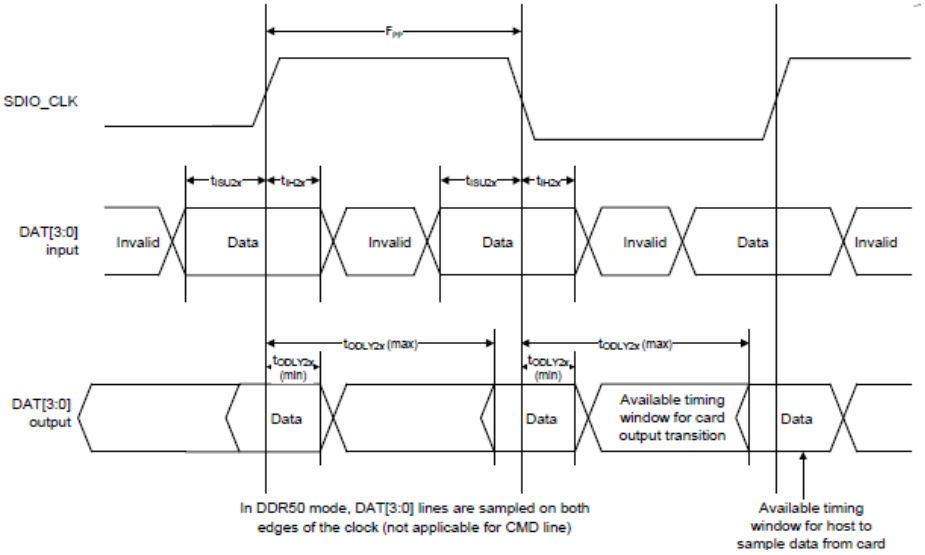


Table 25: SDIO Bus Timing parameters (DDR50 Mode)

Parameter	Symbol	Min	Max	Unit	Comments
Input CMD					
Input setup time	tISU	6	-	ns	Ccard<10pF (1 card)
Input hold time	tIH	0.8	-	ns	Ccard<10pF (1 card)
Output CMD					
Output delay time	tODLY	-	13.7	ns	Ccard<30pF (1 card)
Output hold time	tOH	1.5	-	ns	Ccard<15pF (1 card)
Input DAT					
Input setup time	tISU2x	3	-	ns	Ccard<10pF (1 card)
Input hold time	tIH2x	0.8	-	ns	Ccard<10pF (1 card)
Output DAT					
Output delay time	tODLY2x	-	7.5	ns	Ccard<25pF (1 card)
Output hold time	tOH2x	1.5	-	ns	Ccard<15pF (1 card)

13.5 PCI Express Interface Parameters

Table 26 describes PCI Express Interface Parameters.

Table 26: PCI Express Interface Parameters

Parameter	Symbol	Comments	Min	Typical	Max	Unit
General						
Baud rate	BPS	–	–	5	–	Gbaud
Reference clock peak-to-peak Differential amplitude (a)	VIH (b)	Differential Input High Voltage	150	–	–	mV
	VIL (b)	Differential Input Low Voltage	–	–	–150	mV
	Vcross (c,d,e)	Absolute crossing point Voltage	250	–	550	mV
Receiver						
Differential termination	ZRX-DIFF-DC	Differential termination	80.0	100	120	Ω
DC impedance	ZRX-DC	DC common-mode impedance	40.0	50.0	60.0	Ω
Powered down termination (POS)	ZRX-HIGH-IMP-DCPOS	Power-down or RESET high impedance	100k	–	–	Ω
Powered down termination (NEG)	ZRX-HIGH-IMP-DCNEG	Power-down or RESET high impedance	1k	–	–	Ω
Input voltage	VRX-DIFF p-p	AC coupled, differential p-p	175	–	–	mV
Jitter tolerance	TRX-EYE	Minimum receiver eye width	0.4	–	–	UI
Differential return loss	RLRX-DIFF	Differential return loss	10.0	–	–	dB
Common-mode return loss	RLRX-CM	Common-mode return loss	6	–	–	dB
Unexpected electrical idle enter detect threshold integration time	TRX-IDEL-DET-DIFFENTERTIME	An unexpected electrical idle must be recognized no longer than this time to signal an unexpected idle condition.		–	10.0	Ms
Signal detect threshold	VRX-IDLE-DET-DIFF p-p	Electrical idle detect threshold	65.0	–	175	mV
Transmitter						
Output voltage	VTX-DIFFp-p	Differential p-p, programmable in 16 steps	0.8	–	1200	mV
Output voltage rise time	VTX-RISE	20% to 80%	0.125 (2.5 GT/s) 0.15 (5 GT/s)	–	–	UI
Output voltage fall time	VTX-FALL	80% to 20%	0.125 (2.5 GT/s) 0.15 (5 GT/s)	–	–	UI
RX detection voltage swing	VTX-RCV-DETECT	The amount of voltage change allowed during receiver detection	–	–	600	mV
TX AC peak common mode voltage (5 GT/s)	VTX-CM-AC-PP	TX AC common mode voltage (5 GT/s)	–	–	100100	mV
TX AC peak common mode voltage (2.5 GT/s)	VTX-CM-AC-P	TX AC common mode voltage (2.5 GT/s)	–	–	20.0	mV
Absolute delta of DC common-model voltage during L0 and electrical idle	VTX-CM-DC-ACTIVEIDLE-DELTA	Absolute delta of DC common-model voltage during L0 and electrical idle.	0	–	100	mV
Absolute delta of DC common-model voltage between D+ and D-	VTX-CM-DC-LINEDELTA	DC offset between D+ and D-	0	–	25.0	mV
Electrical idle differential peak output voltage	VTX-IDLE-DIFF-AC-p	Peak-to-peak voltage	0	–	20.0	mV
TX short circuit current	ITX-SHORT	Current limit when TX output is shorted to ground.	–	–	90.0	mA
DC differential TX termination	ZTX-DIFF-DC	Low impedance defined during signaling (parameter is captured for 5.0 GHz by RLTX DIFF)	80.0	–	120	Ω
Differential return loss	RLTX-DIFF	Differential return loss	10 (min) for 0.05: 1.25 GHz	–	–	dB
Common-mode return loss	RLTX-CM	Common-mode return loss	6.0	–	–	dB
TX eye width	TTX-EYE	Minimum TX eye width	0.75	–	–	UI

(a) The reference clock inputs comply with the requirements of PCI Express CEM v2.0.
(b) Measurements taken from differential waveform.
(c) Measurements taken from single ended waveform.
(d) Measurements at crossing point where the instantaneous voltage value of the rising edge REFCLK+ equals the falling edge of REFCLK-.
(e) Refers to the total variations from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for the requirements.

14 Electrical Characteristics

This section describes the electrical characteristics of the Type 2EA module.

14.1 DC/RF Characteristics for IEEE 802.11b - 2.4G

Normal Condition: 25 °C, VBAT = 3.3V, 11 Mbps mode (unless otherwise specified).

Table 27: DC/RF Characteristics for IEEE 802.11b - 2.4 GHz

Items	Contents			
Specification	IEEE 802.11b - 2.4 GHz			
Mode	DSSS / CCK			
Channel Frequency (Spacing)	2412 to 2472 MHz (5 MHz)			
Data Rate	1, 2, 5.5, 11 Mbps			
Current Consumption	**Minimum**	**Typical**	**Maximum**	**Unit**
• Tx Mode		290	400	mA
• Rx Mode		55	100	mA
Transmitter	**Minimum**	**Typical**	**Maximum**	**Unit**
Power Levels	15.5	18	20	dBm
Spectrum Mask Margin				
• 1st side lobes			-30	dBr
• 2nd side lobes			-50	dBr
Power-on/off ramp			2.0	Ms
RF Carrier Suppression	15			dB
Modulation Accuracy			35	%
Frequency Tolerance	-20		20	Ppm
Spurious Emissions (BW = 100 kHz)				
• 30 Hz ≤ f < 1000 MHz			-36	dBm
• 1000 MHz ≤ f < 12750 MHz			-30	dBm
• 1800 MHz < f ≤ 1900 MHz			-47	dBm
• 5150 MHz < f ≤ 5300 MHz			-47	dBm
Receiver	**Minimum**	**Typical**	**Maximum**	**Unit**
Minimum Input Level (FER ≤ 8%)		-85	-76	dBm
Maximum Input Level (FER ≤ 8%)	-10			dBm
Adjacent Channel Rejection (FER ≤ 8%)	35			dB

14.2 DC/RF Characteristics for IEEE 802.11g - 2.4G

Normal Condition: 25 °C, VBAT = 3.3V, 54 Mbps mode (unless otherwise specified).

Table 28: DC/RF Characteristics IEEE 802.11g - 2.4G

Items	Contents			
Specification	IEEE 802.11g - 2.4 GHz			
Mode	OFDM			
Channel Frequency (Spacing)	2412 to 2472 MHz (5 MHz)			
Data Rate	6, 9, 12, 18, 24, 36, 48, 54 Mbps			
Current Consumption	**Minimum**	**Typical**	**Maximum**	**Unit**
• Tx Mode		260	350	mA
• Rx Mode		55	100	mA
Transmitter	**Minimum**	**Typical**	**Maximum**	**Unit**
Power Levels	14.5	17	19	dBm
Spectrum Mask Margin				
• at fc +/- 11 MHz			-20	dBr
• at fc +/- 20 MHz			-28	dBr
• at fc ≥ +/- 30 MHz			-40	dBr
Constellation Error			-25	dB
Frequency Tolerance	-20		20	Ppm
Spurious Emissions (BW = 100 KHz)				
• 30 Hz ≤ f < 1000 MHz			-36	dBm
• 1000 MHz ≤ f < 12750 MHz			-30	dBm
• 1800 MHz < f ≤ 1900 MHz			-47	dBm
• 5150 MHz < f ≤ 5300 MHz			-47	dBm
Receiver	**Minimum**	**Typical**	**Maximum**	**Unit**
Minimum Input Level (PER ≤ 10%)		-74	-65	dBm
Maximum Input Level (PER ≤ 10%)	-20			dBm
Adjacent Channel Rejection (PER ≤ 10%)	-1			dB

14.3 DC/RF Characteristics for IEEE 802.11n – 2.4 GHz

Normal Condition: 25 °C, VBAT = 3.3V, 65 Mbps (MCS7 – HT 20 MHz) mode (unless otherwise specified).

Table 29: DC/RF Characteristics for IEEE 802.11n – 2.4 GHz

Items	Contents			
Specification	IEEE 802.11n – 2.4 GHz			
Mode	OFDM			
Channel Frequency (Spacing)	2412 to 2472 MHz (5 MHz)			
Data Rate	MCS0 – MCS7			
Current Consumption	**Minimum**	**Typical**	**Maximum**	**Unit**
• Tx Mode		250	350	mA
• Rx Mode		55	100	mA
Transmitter	**Minimum**	**Typical**	**Maximum**	**Unit**
Power Levels	13.5	16	18	dBm
Spectrum Mask Margin				
• at fc +/- 11 MHz			-20	dBr
• at fc +/- 20 MHz			-28	dBr
• at fc > +/- 30 MHz			-45	dBr
Constellation Error (Measured at enhanced mode)			-27	dB
Frequency Tolerance	-20		20	Ppm
Spurious Emissions (BW = 100 KHz)				
• 30 Hz ≤ f < 1000 MHz			-36	dBm
• 1000 MHz ≤ f < 12750 MHz			-30	dBm
• 1800 MHz < f ≤ 1900 MHz			-47	dBm
• 5150 MHz < f ≤ 5300 MHz			-47	dBm
Receiver	**Minimum**	**Typical**	**Maximum**	**Unit**
Minimum Input Level (PER ≤ 10%)		-72	-64	dBm
Maximum Input Level (PER ≤ 10%)	-20			dBm
Adjacent Channel Rejection (PER ≤ 10%)	-2			dB

14.4 DC/RF Characteristics for IEEE 802.11ax (HE20 MHz) - 2.4 GHz

Normal Condition: 25 °C, Supply voltage is typical value provided in Section 6, MCS9 mode (unless otherwise specified).

Table 30: DC/RF Characteristics for IEEE 802.11ax (HE20 MHz) - 2.4 GHz

Items	Contents			
Specification	IEEE 802.11ax - 2.4 GHz			
Mode	OFDM			
Channel Frequency (Spacing)	2412 to 2472 MHz (5 MHz)			
Data Rate	MCS0 – MCS11			
Current Consumption (Total power consumption/3.85v)	**Minimum**	**Typical**	**Maximum**	**Unit**
• Tx Mode (Power setting: 12 dBm)		200	280	mA
• Rx Mode		55	100	mA
Transmitter	**Minimum**	**Typical**	**Maximum**	**Unit**
Power Levels (Power setting: 12 dBm)	9.5	12	14	dBm
Spectrum Mask Margin				
• at fc +/- 10.5 MHz			-20	dBr
• at fc +/- 20 MHz			-28	dBr
• at fc > +/- 30 MHz			-40	dBr
Constellation Error (Measured at full packet channel estimation)			-32	dB
Spurious Emissions (BW = 100 KHz) (With external filter)				
• 30 Hz - 1000 MHz			-36	dBm
• 1000 MHz - 12500 MHz			-30	dBm
• 1800 MHz - 1900 MHz			-47	dBm
• 5150 MHZ - 5300 MHz			-47	dBm
Receiver (PER< 10%, LDPC Enabled)	**Minimum**	**Typical**	**Maximum**	**Unit**
Minimum Input Level (PER ≤ 10%)		-61	-52	dBm
Maximum Input Level (PER ≤ 10%)	-20			dBm
Adjacent Channel Rejection (PER ≤ 10%)	-14			dB

14.5 DC/RF Characteristics for IEEE 802.11a - 5 GHz

Normal Condition: 25 °C, VBAT = 3.3V, 54 Mbps mode (unless otherwise specified).

Table 31: DC/RF Characteristics for IEEE 802.11a - 5 GHz

Items	Contents			
Specification	IEEE 802.11a - 5 GHz			
Mode	OFDM			
Channel Frequency (Spacing)	5180 to 5320 MHz (20 MHz), 5500 to 5720 MHz (20 MHz), 5745 to 5825 MHz (20 MHz)			
Data Rate	6, 9, 12, 18, 24, 36, 48, 54 Mbps			
Current Consumption	**Minimum**	**Typical**	**Maximum**	**Unit**
• Tx Mode		360	500	mA
• Rx Mode		55	100	mA
Transmitter	**Minimum**	**Typical**	**Maximum**	**Unit**
Power Levels	14	16	18	dBm
Spectrum Mask				
• at fc +/- 11 MHz			-20	dBr
• at fc +/- 20 MHz			-28	dBr
• at fc ≥ +/- 30 MHz			-40	dBr
Constellation Error			-25	dB
Frequency Tolerance	-20		20	ppm
Spurious Emissions (BW = 100 KHz)				
• 30 Hz ≤ f < 1000 MHz			-36	dBm
• 1000 MHz ≤ f < 26000 MHz			-30	dBm
Receiver	**Minimum**	**Typical**	**Maximum**	**Unit**
Minimum Input Level (PER ≤ 10%)		-73	-65	dBm
Maximum Input Level (PER ≤ 10%)	-30			dBm
Adjacent Channel Rejection (PER ≤ 10%)	-2			dB

14.6 DC/RF Characteristics for IEEE 802.11n (HT20 MHz) - 5 GHz

Normal Condition: 25 °C, VBAT = 3.3V, 65 Mbps (MCS7 - HT20 MHz) Mode (unless otherwise specified).

Table 32: DC/RF Characteristics for IEEE 802.11n (HT20 MHz) - 5 GHz

Items	Contents			
Specification	IEEE 802.11n - 5 GHz			
Mode	OFDM			
Channel Frequency (Spacing)	5180 to 5320 MHz (20 MHz), 5500 to 5720 MHz (20 MHz), 5745 to 5825 MHz (20 MHz)			
Data Rate	MCS0 - MCS7			
Current Consumption	**Minimum**	**Typical**	**Maximum**	**Unit**
• Tx Mode		320	450	mA
• Rx Mode		55	100	mA
Transmitter	**Minimum**	**Typical**	**Maximum**	**Unit**
Power Levels	12	14	16	dBm
Spectrum Mask Margin				
• at fc +/- 11 MHz			-20	dBr
• at fc +/- 20 MHz			-28	dBr
• at fc ≥ +/- 30 MHz			-40	dBr
Constellation Error (Measured at enhanced mode)			-27	dB
Frequency Tolerance	-20		20	ppm
Spurious Emissions (BW = 100 KHz)				
• 30 Hz ≤ f < 1000 MHz			-36	dBm
• 1000 MHz ≤ f < 26000 MHz			-30	dBm
Receiver	**Minimum**	**Typical**	**Maximum**	**Unit**
Minimum Input Level (PER ≤ 10%)		-72	-64	dBm
Maximum Input Level (PER ≤ 10%)	-30			dBm
Adjacent Channel Rejection (PER ≤10%)	-2			dB

14.7 DC/RF Characteristics for IEEE 802.11n (HT40 MHz) - 5 GHz

Normal Condition: 25 °C, VBAT = 3.3V, 135 Mbps (MCS7 - HT40 MHz) mode (unless otherwise specified).

Table 33: DC/RF Characteristics for IEEE 802.11n (HT40 MHz) - 5 GHz

Items	Contents			
Specification	IEEE 802.11n - 5 GHz			
Mode	OFDM			
Channel Frequency (Spacing)	5510 to 5310 MHz (40 MHz), 5510 to 5710 MHz (40 MHz), 5755 to 5795 MHz (40 MHz)			
Data Rate	MCS0 - MCS7			
Current Consumption	**Minimum**	**Typical**	**Maximum**	**Unit**
• Tx Mode		340	450	mA
• Rx Mode		55	100	mA
Transmitter	**Minimum**	**Typical**	**Maximum**	**Unit**
Power Levels	12	14		dBm
Spectrum Mask Margin				
• at fc +/- 21 MHz			-20	dBr
• at fc +/- 40 MHz			-28	dBr
• at fc ≥ +/- 60 MHz			-40	dBr
Constellation Error (Measured at enhanced mode)			-27	dB
Frequency Tolerance	-20		20	ppm
Spurious Emissions (BW = 100 kHz)				
• 30 Hz ≤ f < 1000 MHz			-36	dBm
• 1000 MHz ≤ f < 26000 MHz	-	-	-30	dBm
Receiver	**Minimum**	**Typical**	**Maximum**	**Unit**
Minimum Input Level (PER ≤ 10%)		-69	-61	dBm
Maximum Input Level (PER ≤ 10%)	-30			dBm
Adjacent Channel Rejection (PER ≤ 10%)	2			dB

14.8 DC/RF Characteristics for IEEE 802.11ac (VHT40 MHz) - 5 GHz

Normal Condition: 25 °C, VBAT = 3.3V, 180 Mbps (MCS9 - VHT40 MHz) mode (unless otherwise specified).

Table 34: DC/RF Characteristics for IEEE 802.11ac (VHT40 MHz) - 5 GHz

Items	Contents			
Specification	IEEE 802.11ac - 5 GHz			
Mode	OFDM			
Channel Frequency (Spacing)	5510 to 5310 MHz (40 MHz), 5510 to 5710 MHz (40 MHz), 5755 to 5795 MHz (40 MHz)			
Data Rate	MCS0 - MCS9			
Current Consumption	**Minimum**	**Typical**	**Maximum**	**Unit**
• Tx Mode		310	450	mA
• Rx Mode		55	100	mA
Transmitter	**Minimum**	**Typical**	**Maximum**	**Unit**
Power Levels	10	12	14	dBm
Spectrum Mask Margin				
• at fc +/- 21 MHz			-20	dBr
• at fc +/- 40 MHz			-28	dBr
• at fc ≥ +/- 60 MHz			-40	dBr
Constellation Error (Measured at enhanced mode)			-32	dB
Frequency Tolerance	-20		20	ppm
Spurious Emissions (BW = 100 kHz)				
• (a) 30 Hz ≤ f < 1000 MHz			-36	dBm
• (b) 1000 MHz ≤ f < 26000 MHz			-30	dBm
Receiver	**Minimum**	**Typical**	**Maximum**	**Unit**
Minimum Input Level (PER ≤ 10%)		-63	-54	dBm
Maximum Input Level (PER ≤ 10%)	-30			dBm
Adjacent Channel Rejection (PER ≤ 10%)	-9			dB

14.9 DC/RF Characteristics for IEEE 802.11ac (VHT80 MHz) - 5 GHz

Normal Condition: 25 °C, VBAT = 3.3V, 390 Mbps (MCS9 - HT80 MHz) mode (unless otherwise specified).

Table 35: DC/RF Characteristics for IEEE 802.11ac (VHT80 MHz) - 5 GHz

Items	Contents			
Specification	IEEE 802.11ac - 5 GHz			
Mode	OFDM			
Channel Frequency (Spacing)	5210 to 5290 MHz (80 MHz), 5530 to 5690 MHz (80 MHz), 5775 MHz (80 MHz)			
Data Rate	MCS0 - MCS9			
Current Consumption (Total power consumption/3.85v)	**Minimum**	**Typical**	**Maximum**	**Unit**
• Tx Mode		330	450	mA
• Rx Mode		55	100	mA
Transmitter	**Minimum**	**Typical**	**Maximum**	**Unit**
Power Levels	10	12	14	dBm
Spectrum Mask Margin				
• at fc +/- 41 MHz			-20	dBr
• at fc +/- 80 MHz			-28	dBr
• at fc ≥ +/- 120 MHz			-40	dBr
Constellation Error (Measured at enhanced mode)			-32	dB
Spurious Emissions (BW = 100 kHz)				
• 30 Hz ≤ f < 1000 MHz			-36	dBm
• 1000 MHz ≤ f < 26000 MHz			-30	dBm
Receiver	**Minimum**	**Typical**	**Maximum**	**Unit**
Minimum Input Level (PER ≤ 10%)		-60	-51	dBm
Maximum Input Level (PER ≤ 10%)	-30			dBm
Adjacent Channel Rejection (PER ≤ 10%)	-9			dB

14.10 DC/RF Characteristics for IEEE 802.11ax (HE20 MHz) - 5 GHz

Normal Condition: 25 °C, VBAT = 3.3V, MCS11 mode (unless otherwise specified).

Table 36: DC/RF Characteristics for IEEE 802.11ax (HE20 MHz) - 5 GHz

Items	Contents			
Specification	IEEE 802.11ax - 5 GHz			
Mode	OFDM			
Channel Frequency (Spacing)	5180 to 5320 MHz (20 MHz), 5500 to 5720 MHz (20 MHz), 5745 to 5825 MHz (20 MHz)			
Data Rate	MCS0 – MCS11			
Current Consumption	**Minimum**	**Typical**	**Maximum**	**Unit**
• Tx Mode (Power setting: 9 dBm)		270	340	mA
• Rx Mode		55	100	mA
Transmitter	**Minimum**	**Typical**	**Maximum**	**Unit**
Power Levels	7	9	11	dBm
Spectrum Mask				
• at fc +/- 10.25 MHz			-20	dBr
• at fc +/- 20 MHz			-28	dBr
• at fc ≥ +/- 30 MHz			-40	dBr
Constellation Error (Measured at full packet channel estimation)			-35	dB
Spurious Emissions (BW = 100 kHz) (With external filter)				
• 30 MHz -1 GHz			-36	dBm
• 1GHz - 26 GHz			-30	dBm
Receiver (PER< 10%, LDPC enabled)	**Minimum**	**Typical**	**Maximum**	**Unit**
Minimum Input Level (PER ≤ 10%)		-60	-52	dBm
Maximum Input Level (PER ≤ 10%)	-30			dBm
Adjacent Channel Rejection (PER ≤ 10%)	-14			dB

14.11 DC/RF Characteristics for IEEE 802.11ax (HE40 MHz) - 5 GHz

Normal Condition: 25 °C, VBAT = 3.3V, MCS11 mode (unless otherwise specified).

Table 37: DC/RF Characteristics for IEEE 802.11ax (HE40 MHz) - 5 GHz

Items	Contents			
Specification	IEEE 802.11ax - 5 GHz			
Mode	OFDM			
Channel Frequency (Spacing)	5510 to 5310 MHz (40 MHz), 5510 to 5710 MHz (40 MHz), 5755 to 5795 MHz (40 MHz)			
Data Rate	MCS0 – MCS11			
Current Consumption (Total power consumption/3.85v)	**Minimum**	**Typical**	**Maximum**	**Unit**
• Tx Mode (Power setting: 9 dBm)		280	350	mA
• Rx Mode		55	100	mA
Transmitter	**Minimum**	**Typical**	**Maximum**	**Unit**
Power Levels	7	9	11	dBm
Spectrum Mask Margin				
• at fc +/- 20.5 MHz			-20	dBr
• at fc +/- 40 MHz			-28	dBr
• at fc ≥ +/- 60 MHz			-40	dBr
Constellation Error (Measured at full packet channel estimation)			-35	dB
Spurious Emissions (BW = 100 kHz) (With external filter)				
• 30 MHz -1 GHz			-36	dBm
• 1 GHz - 26 GHz			-30	dBm
Receiver (PER< 10%, LDPC enabled)	**Minimum**	**Typical**	**Maximum**	**Unit**
Minimum Input Level (PER ≤ 10%)		-57	-49	dBm
Maximum Input Level (PER ≤ 10%)	-30			dBm
Adjacent Channel Rejection (PER ≤ 10%)	-14			dB

14.12 DC/RF Characteristics for IEEE 802.11ax (HE80 MHz) - 5 GHz

Normal Condition: 25 °C, VBAT = 3.3V, MCS11 mode (unless otherwise specified).

Table 38: DC/RF Characteristics for IEEE 802.11ax (HE80 MHz) - 5 GHz

Items	Contents			
Specification	IEEE 802.11ax - 5 GHz			
Mode	OFDM			
Channel Frequency (Spacing)	5210 to 5290 MHz (80 MHz), 5530 to 5690 MHz (80 MHz), 5775 MHz (80 MHz)			
Data Rate	MCS0 – MCS11			
Current Consumption (Total power consumption/3.85v)	**Minimum**	**Typical**	**Maximum**	**Unit**
• Tx Mode (Power setting: 9 dBm)		290	370	mA
• Rx Mode		55	100	mA
Transmitter	**Minimum**	**Typical**	**Maximum**	**Unit**
Power Levels	7	9	11	dBm
Spectrum Mask				
• at fc +/- 40.5 MHz			-20	dBr
• at fc +/- 80 MHz			-28	dBr
• at fc ≥ +/- 120 MHz			-40	dBr
Constellation Error (Measured at full packet channel estimation)			-35	dB
Spurious Emissions (BW = 100 kHz) (With external filter)				
• 30 MHz -1 GHz			-36	dBm
• 1 GHz - 26 GHz			-30	dBm
Receiver	**Minimum**	**Typical**	**Maximum**	**Unit**
Minimum Input Level (PER ≤ 10%)			-46	dBm
Maximum Input Level (PER ≤ 10%)	-30			dBm
Adjacent Channel Rejection (PER ≤ 10%)	2			dB

14.13 DC/RF Characteristics for IEEE 802.11a - 6 GHz

Normal Condition: 25 °C, VBAT = 3.3V, 24 Mbps mode (unless otherwise specified).

Table 39: DC/RF Characteristics for IEEE 802.11a - 6 GHz

Items	Contents			
Specification	IEEE 802.11a - 6 GHz			
Mode	OFDM			
Channel Frequency (Spacing)	5955 to 7115 MHz (20 MHz)			
Data Rate	6, 9, 12, 18, 24 Mbps			
Current Consumption	**Minimum**	**Typical**	**Maximum**	**Unit**
• Tx Mode		260	340	mA
• Rx Mode		55	100	mA
Transmitter	**Minimum**	**Typical**	**Maximum**	**Unit**
Power Levels	6.5	9	11	dBm
Spectrum Mask Margin				
• fc +/- 11 MHz			-20	dBr
• at fc +/- 20 MHz			-28	dBr
• at fc ≥ +/- 30 MHz			-40	dBr
Constellation Error			-25	dB
Frequency Tolerance	-20		20	ppm
Spurious Emissions (BW = 100 kHz)				
• 30 Hz ≤ f < 1000 MHz			-36	dBm
• 1000 MHz ≤ f < 26000 MHz			-30	dBm
Receiver	**Minimum**	**Typical**	**Maximum**	**Unit**
Minimum Input Level (PER ≤ 10%)			-74	dBm
Maximum Input Level (PER ≤ 10%)	-30			dBm
Adjacent Channel Rejection (PER ≤ 10%)	8			dB

14.14 DC/RF Characteristics for IEEE 802.11ax (HE20 MHz) - 6 GHz

Normal Condition: 25 °C, VBAT =3.3V, MCS11 mode (unless otherwise specified).

Table 40: DC/RF Characteristics for IEEE 802.11ax (HE20 MHz) - 6 GHz

Items	Contents			
Specification	IEEE 802.11ax - 6 GHz			
Mode	OFDM			
Channel Frequency (Spacing)	5955 to 7115 MHz (20 MHz)			
Data Rate	MCS0 – MCS11			
Current Consumption (Total power consumption/3.85v)	**Minimum**	**Typical**	**Maximum**	**Unit**
• Tx Mode (Power setting : 9 dBm)		260	340	mA
• Rx Mode		55	100	mA
Transmitter	**Minimum**	**Typical**	**Maximum**	**Unit**
Power Levels	6.5	9	11	dBm
Spectrum Mask Margin				
• at fc +/- 10.25 MHz			-20	dBr
• at fc +/- 20 MHz			-28	dBr
• at fc ≥ +/- 30 MHz			-40	dBr
Constellation Error (Measured at full packet channel estimation)			-35	dB
Spurious Emissions (BW = 100 kHz) (With external filter)				
• 30 MHz -1 GHz			-36	dBm
• 1 GHz - 26 GHz			-30	dBm
Receiver (PER< 10%, LDPC enabled)	**Minimum**	**Typical**	**Maximum**	**Unit**
Minimum Input Level (PER ≤ 10%)		-58	-52	dBm
Maximum Input Level (PER ≤ 10%)	-30			dBm
Adjacent Channel Rejection (PER ≤ 10%)	-14			dB

14.15 DC/RF Characteristics for IEEE 802.11ax (HE40 MHz) - 6 GHz

Normal Condition: 25 °C, VBAT = 3.3V, MCS11 mode (unless otherwise specified).

Table 41: DC/RF Characteristics for IEEE 802.11ax (HE40 MHz) - 6 GHz

Items	Contents			
Specification	IEEE 802.11ax - 6 GHz			
Mode	OFDM			
Channel Frequency (Spacing)	5965 to 7085 MHz (40 MHz)			
Data Rate	MCS0 – MCS11			
Current Consumption (Total power consumption/3.85v)	**Minimum**	**Typical**	**Maximum**	**Unit**
• Tx Mode (Power setting: 9 dBm)		260	350	mA
• Rx Mode		55	100	mA
Transmitter	**Minimum**	**Typical**	**Maximum**	**Unit**
Power Levels	6.5	9	11	dBm
Spectrum Mask				
• at fc +/- 20.5 MHz			-20	dBr
• at fc +/- 40 MHz			-28	dBr
• at fc > +/-60 MHz			-40	dBr
Constellation Error (Measured at full packet channel estimation)			-35	dB
Spurious Emissions (BW = 100 kHz) (With external filter)				
• 30 MHz -1 GHz			-36	dBm
• 1 GHz - 26 GHz			-30	dBm
Receiver (PER< 10%, LDPC enabled)	**Minimum**	**Typical**	**Maximum**	**Unit**
Minimum Input Level (PER ≤ 10%)		-56	-49	dBm
Maximum Input Level (PER ≤ 10%)	-30			dBm
Adjacent Channel Rejection (PER ≤ 10%)	-14			dB

14.16 DC/RF Characteristics for IEEE 802.11ax (HE80 MHz) - 6 GHz

Normal Condition: 25 °C, VBAT = 3.3V, MCS11 mode (unless otherwise specified).

Table 42: DC/RF Characteristics for IEEE 802.11ax (HE40 MHz) - 6 GHz

Items	Contents			
Specification	IEEE 802.11ax - 6 GHz			
Mode	OFDM			
Channel Frequency (Spacing)	5985 to 7025 MHz (80 MHz)			
Data Rate	MCS0 – MCS11			
Current Consumption (Total power consumption/3.85v)	**Minimum**	**Typical**	**Maximum**	**Unit**
Tx Mode (Power setting: 9 dBm)		270	370	mA
Rx Mode		55	100	ma
Transmitter	**Minimum**	**Typical**	**Maximum**	**Unit**
Power Levels (Power setting: 9 dBm)	6.5	9	11	dBm
Spectrum Mask				
• at fc +/- 40.5 MHz			-20	dBr
• at fc +/- 80 MHz			-28	dBr
• at fc ≥ +/- 120 MHz			-40	dBr
Constellation Error (Measured at full packet channel estimation)			-35	dB
Spurious Emissions (BW = 100 kHz) (With external filter)				
• 30 MHz -1 GHz			-36	dBm
• 1 GHz - 26 GHz			-30	dBm
Receiver (PER< 10%, LDPC enabled)	**Minimum**	**Typical**	**Maximum**	**Unit**
Minimum Input Level (PER ≤ 10%)		-54	-46	dBm
Maximum Input Level (PER ≤ 10%)	-30			dBm
Adjacent Channel Rejection (PER ≤ 10%)	-14			dB

14.17 DC/RF Characteristics for Bluetooth

Normal conditions: 25 °C, VBAT = 3.3V

Table 43: DC/RF Characteristics for Bluetooth

Items	Contents			
Bluetooth Specification (Power Class)	Version 5.3 (Class 1.5)			
Channel Frequency (Spacing)	2402 to 2480 MHz (1 MHz)			
Current Consumption	**Minimum**	**Typical**	**Maximum**	**Unit**
• DH5 Packet 50% Rx/Tx slot duty cycle		34	45	mA
• 2DH5 Packet 50% Rx/Tx slot duty cycle		35	45	mA
• 3DH5 Packet 50% Rx/Tx slot duty cycle		36	45	mA
Transmitter	**Minimum**	**Typical**	**Maximum**	**Unit**
Output Power (at DH5)	5	8	10.5	dBm
Output Power (at 2DH5, 3DH5)	1	4	6.5	
Frequency Range	2402		2480	MHz
20 dB bandwidth			1	MHz
Adjacent Channel Power[3]				
• [M-N] = 2			-20	dBm
• [M-N] ≥ 3			-40	dBm
Modulation Characteristics				
• Modulation $\Delta f1_{avg}$	140		175	kHz
• Modulation $\Delta f2_{max}$	115			kHz
• Modulation $\Delta f2_{avg}$ / $\Delta f1_{avg}$	0.8			
Carrier Frequency Drift				
• 1slot	-25		+25	kHz
• 3slot / 5slot	-40		+40	kHz
• Maximum drift rate	-20		+20	kHz/50µs
EDR Relative Power	-4		+1	dB
EDR Carrier Frequency Stability and Modulation Accuracy				
• ωi	-75		+75	kHz
• ωi+ωo	-75		+75	kHz
• ωo	-10		+10	kHz
• RMS DEVM (DQPSK)			20	%
• Peak DEVM (DQPSK)			35	%
• 99% DEVM (DQPSK)			30	%
• RMS DEVM (8DPSK)			13	%
• Peak DEVM (8DPSK)			25	%
• 99% DEVM (8DPSK)			20	%
Spurious Emissions (BW = 100 kHz)				
• 30 Hz ≤ f < 1000 MHz			-36	dBm
• 1000 MHz ≤ f < 12750 MHz			-30	dBm
• 1800 MHz < f ≤ 1900 MHz			-47	dBm
• 5150 MHz < f ≤ 5300 MHz			-47	dBm
Receiver	**Minimum**	**Typical**	**Maximum**	**Unit**
BR (DFSK) Sensitivity (BER < 0.1%)		-90	-70	dBm
Maximum Input Level (BER < 0.1%)	-20			dBm
EDR (8DPSK) Sensitivity (BER ≤ 0.007%)		-87	-70	dBm

[3] Up to three spurious responses within Bluetooth limits are allowed.

14.18 DC/RF Characteristics for Bluetooth (LE)

Normal Conditions: 25 °C, VBAT = 3.3V

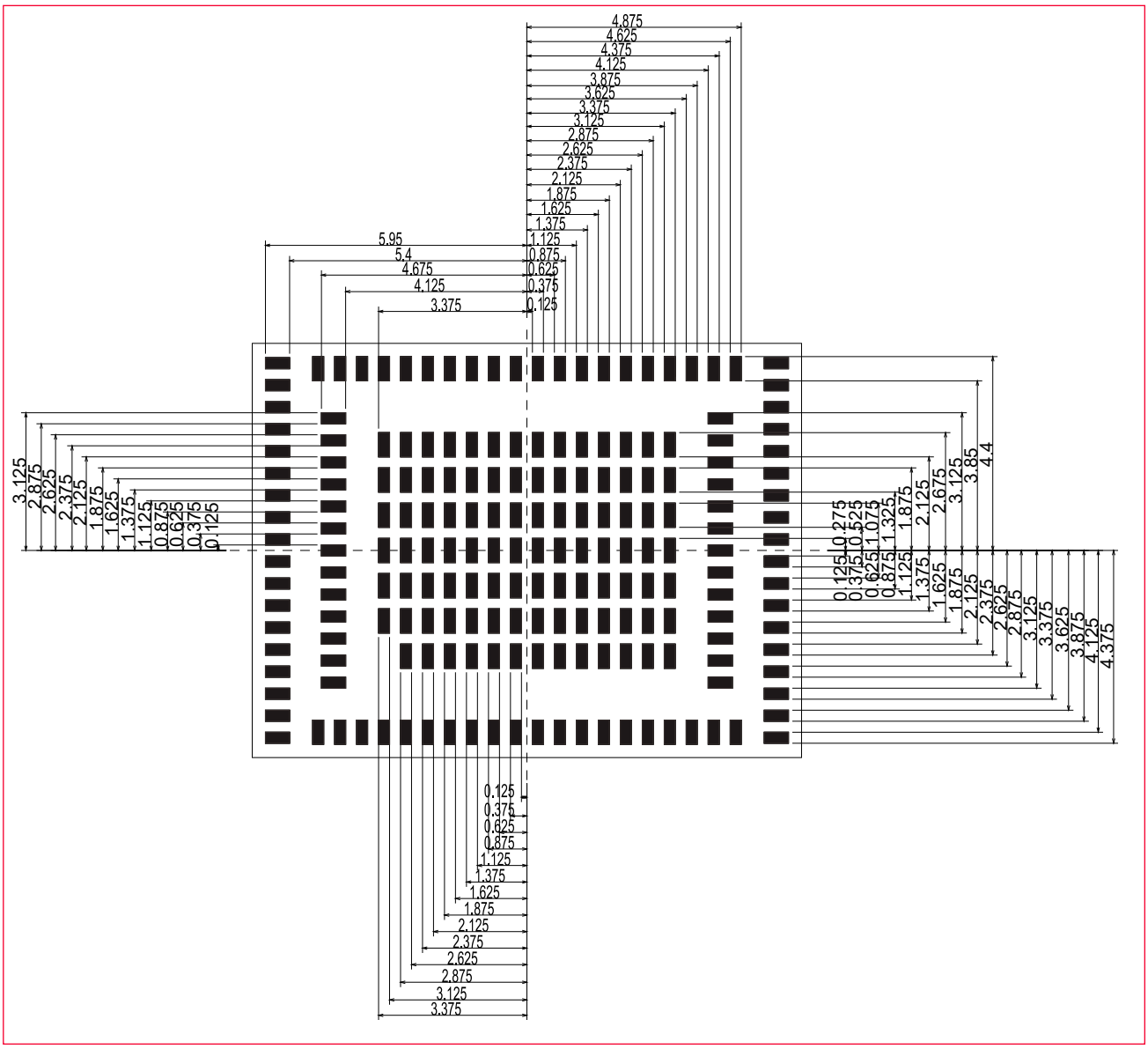
Table 44: DC/RF Characteristics for Bluetooth (LE)

Items	Contents			
Bluetooth Specification (Power Class)	Version 5.3 (LE)			
Channel Frequency (Spacing)	2402 to 2480 MHz (2 MHz)			
Number of RF Channel	40			
Current Consumption	**Minimum**	**Typical**	**Maximum**	**Unit**
• Tx Mode		26	40	mA
• Rx Mode				mA
Item/Condition	**Minimum**	**Typical**	**Maximum**	**Unit**
Center Frequency	2402		2480	MHz
Channel Spacing		2		MHz
Number of RF channel		40		
Output Power	5	8	10.5	dBm
Modulation Characteristics				
• $\Delta f1_{avg}$	225		275	kHz
• $\Delta f2_{max}$ (at 99.9%)	185			kHz
• $\Delta f2_{avg} / \Delta f1_{avg}$	0.8			
Carrier Frequency Offset and Drift				
• Frequency Offset			150	kHz
• Frequency Drift			50	kHz
• Drift Rate			20	kHz
Receiver Sensitivity (PER < 30.8%)		-96	-70	dBm
Maximum Input Signal Level (PER < 30.8%)	-10			dBm
PER Report Integrity (-30 dBm input)	50		65.4	%

15 Land Pattern (Top View)

Figure 24 shows the top view of Type 2EA land pattern.

Figure 24: Land Pattern (Top View)



16 Radio Regulatory Certification by Country for LBEE5XV2EA

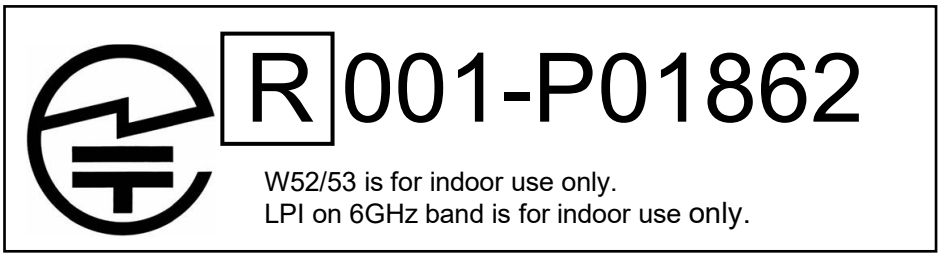
This section includes regulatory certification information / user guide of the following regions:

- Japan
- FCC
- ISED
- Europe

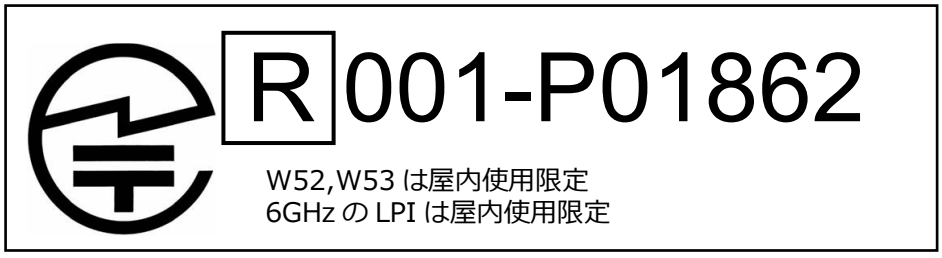
16.1 Japan

- **Application Model Name:** LBEE5XV2EA
- **Certification Number:** 001-P01862

English



Japanese



This module is a product that has been authorized construction design certification based on the following certificate of construction type.

- In the 5 GHz frequency band, three types of 5.2 GHz / 5.3 GHz / 5.6 GHz bands (W52 / W53 / W56) can be used.
- Outdoor use of the 5.2 GHz / 5.3 GHz band wireless LAN (W52 / W53) is prohibited by the Certificate of Construction Type.
- W53 / W56 for STA function only.
- Outdoor use of the LPI setting of 6GHz frequency band is prohibited by the Certificate of Construction Type, but outdoor use is allowed with the VLP setting.

The end product or user manual is recommended to describe all the contents shown below.

- This product has built-in specified radio equipment which received construction design certification (certification number: 001-P01862) based on the Certificate of Construction.
- The W52 / W53 in the 5 GHz band is prohibited from outdoor use under the Japanese Certificate of Construction Type.
- The LPI setting of 6GHz frequency band is prohibited from outdoor use under the Japanese Certificate of Construction Type.

16.2 FCC

Unfinished

16.3 ISED

Unfinished

16.4 Europe

Unfinished

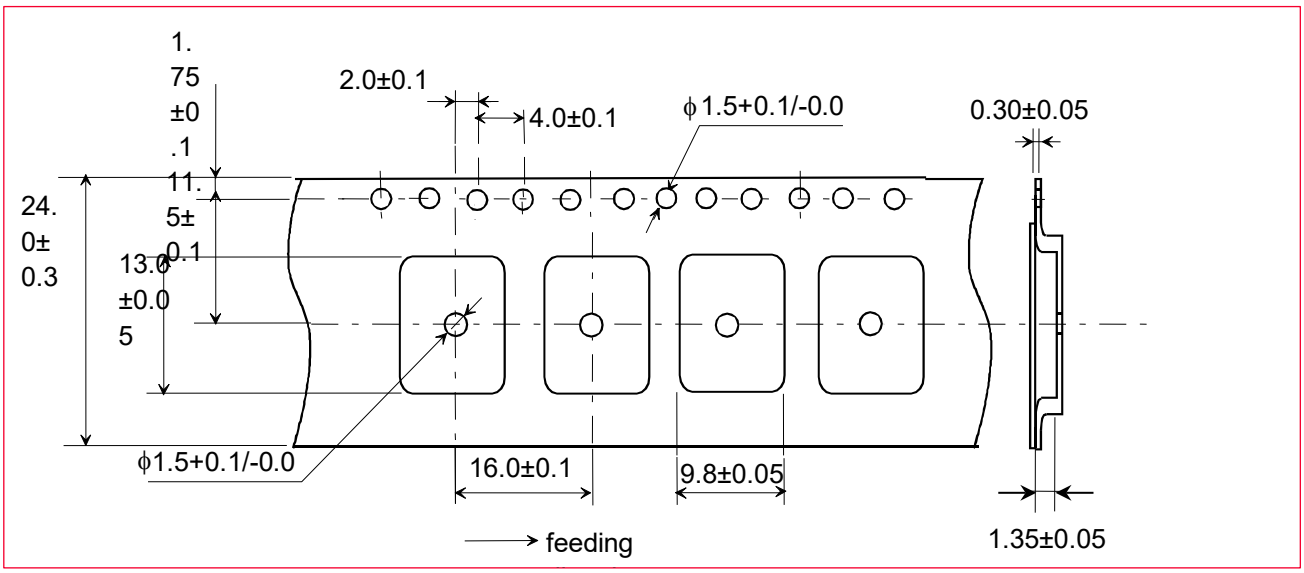
17 Tape And Reel Packing

This section describes the tape and reel packing, i.e., the dimensions of the plastic tape, reel and taping diagrams.

17.1 Dimensions of Tape

Figure 25 shows the dimensions of the plastic tape.

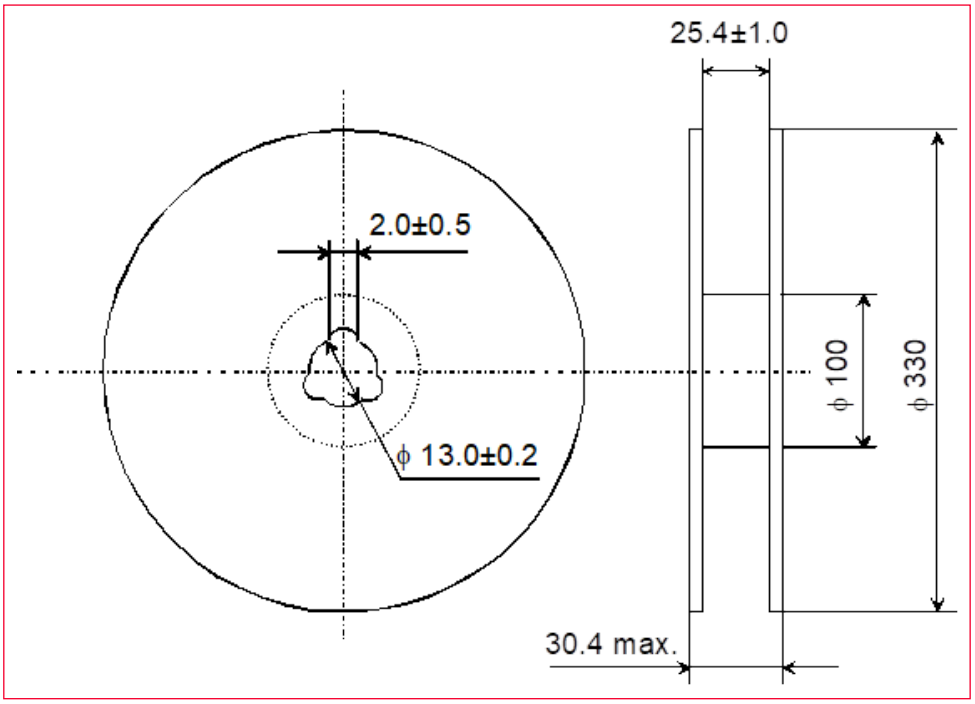
Figure 25: Dimensions of Tape (Plastic Tape)



17.2 Dimensions of Reel

Figure 26 shows the dimensions of reel.

Figure 26: Dimensions of Reel



17.3 Taping Diagrams

Figure 27 shows the taping diagrams.

Figure 27: Taping Diagrams

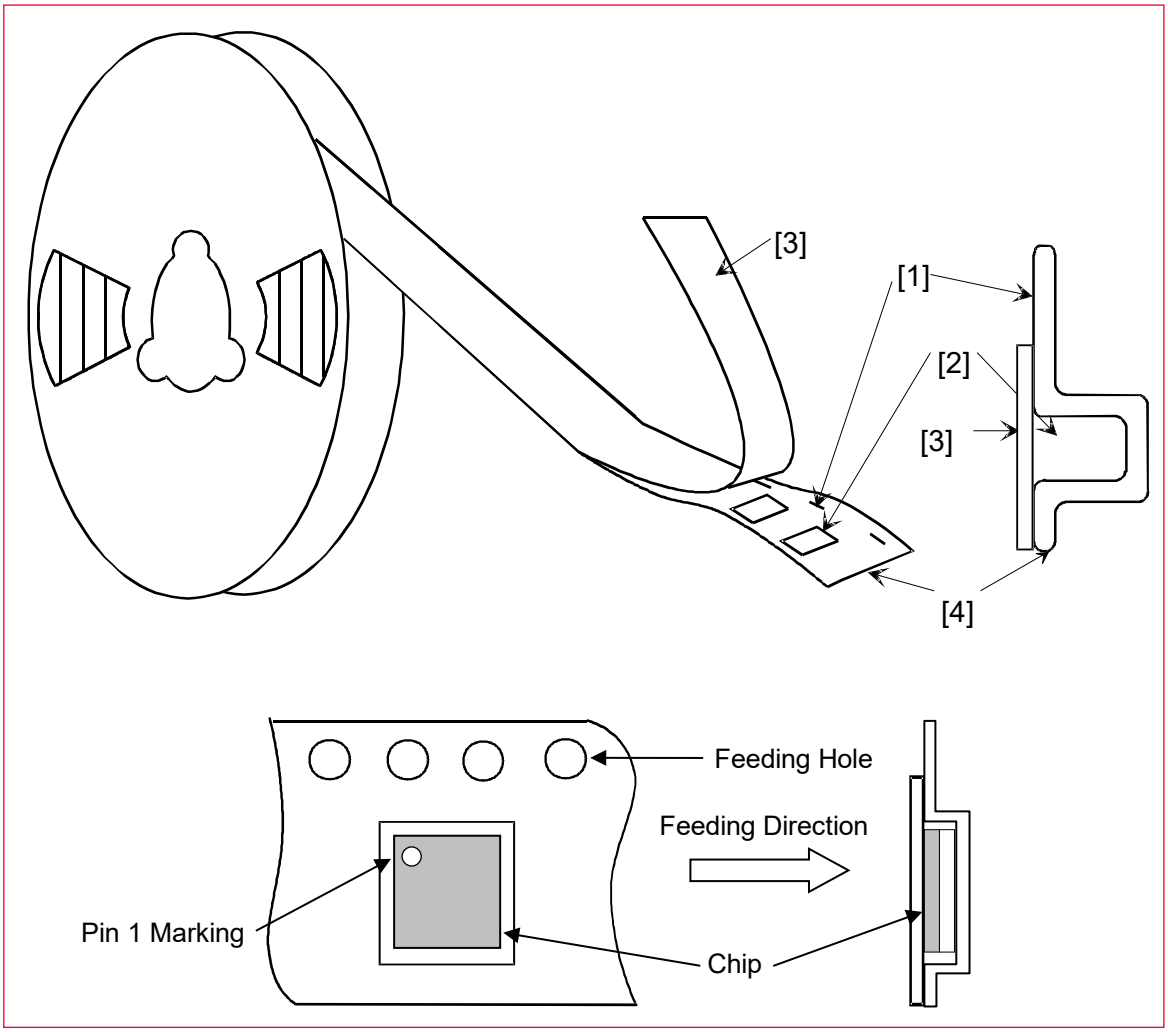


Table 45 describes the taping specifications.

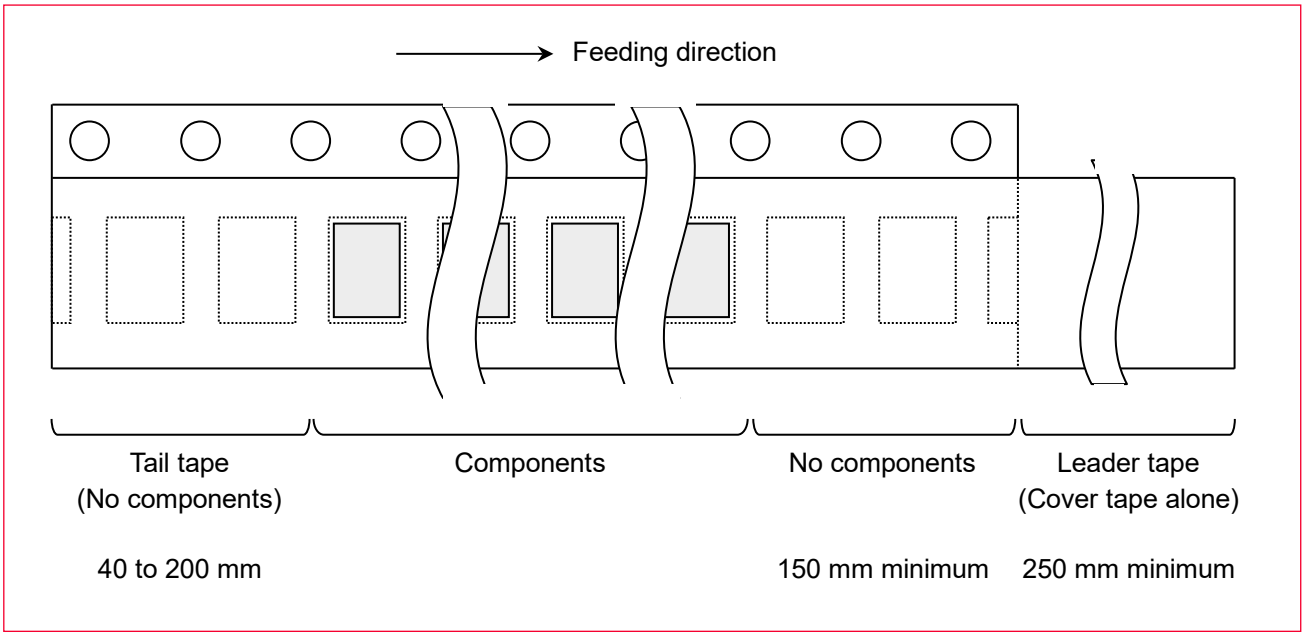
Table 45: Taping Specifications

Mark	Description
1	Feeding Hole: As specified in Dimensions of Tape (Plastic Tape)
2	Hole for chip: As specified in Dimensions of Tape (Plastic Tape)
3	Cover tape: 62 µm in thickness
4	Base tape: As specified in Dimensions of Tape (Plastic Tape)

17.4 Leader and Tail Tape

Figure 28 shows the leader and tail tape.

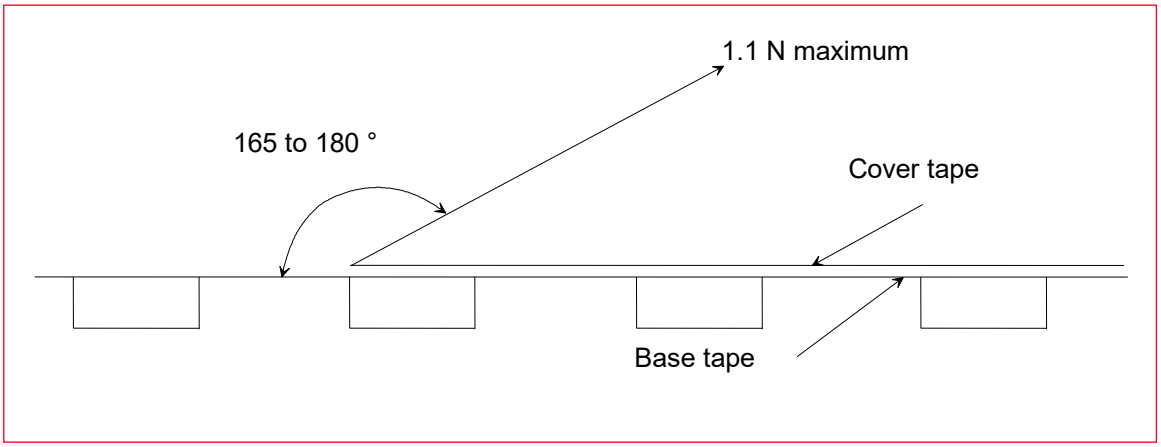
Figure 28: Leader and Tail Tape



- The tape for chips is wound clockwise, the feeding holes to the right side as the tape is pulled toward the user.
- The cover tape and base tape are not adhered at no components area for 250 mm minimum.
- Tear off strength against pulling of cover tape: 5 N minimum.
- Packaging unit: 1000 pcs/reel
- Material
  - Base tape: Plastic
  - Reel: Plastic
- Cover tape, cavity tape and reel are made the anti-static processing.
- Peeling of force: 1.1 N maximum in the direction of peeling as shown below.

Figure 29 shows the peeling off force.

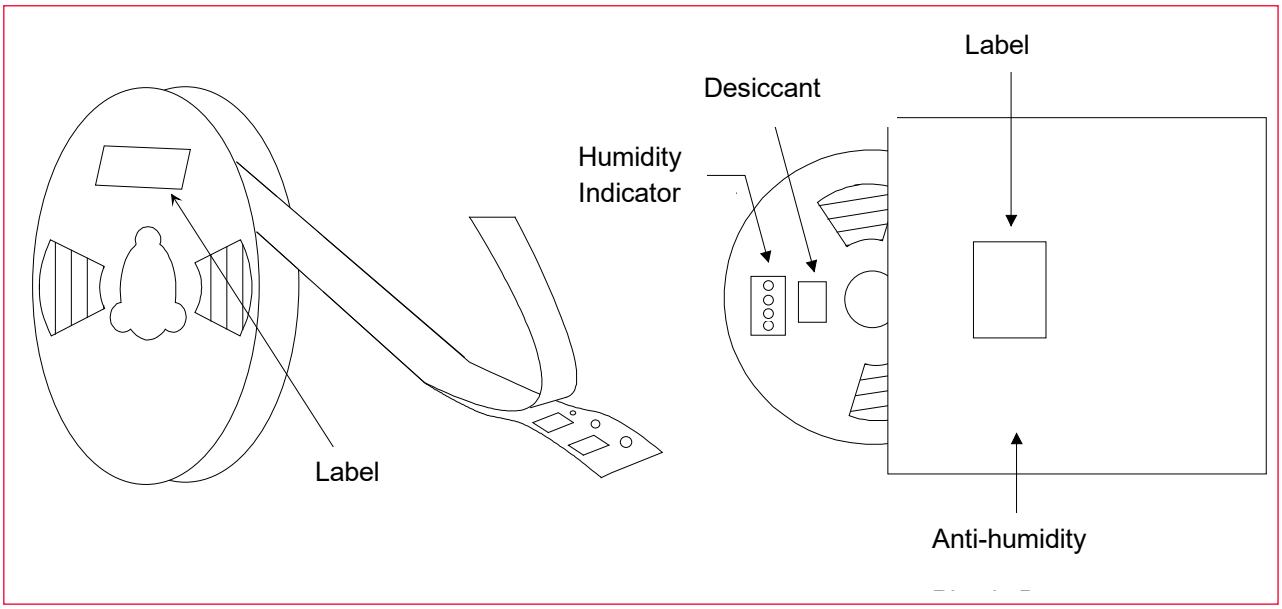
Figure 29: Peeling Off Force



17.5 Packaging (Humidity Proof Packing)

Figure 30 shows the packaging.

Figure 30: Packaging



Tape and reel must be sealed with the anti-humidity plastic bag. The bag contains the desiccant and the humidity indicator.

18 Notice

18.1 Storage Conditions

Please use this product within 6 months after receipt.

- The product *must be* stored without opening the packing under the ambient temperature from 5 to 35 °C and humidity from 20 ~ 70 %RH.

Packing materials, in particular, may be deformed at the temperature over 40 °C

- The solderability of the product left idle for more than 6 months after receipt needs to be confirmed before it is used.
- The product *must be* stored in noncorrosive gas (Cl_2, NH_3, SO_2, NO_X, etc.).
- Any excess mechanical shock including, but not limited to, sticking the packing materials by sharp object, and dropping the product, *must not be* applied as that will damage the packing materials.

This product is applicable to MSL3 (Based on JEDEC Standard J-STD-020)

- After the packing is opened, the product *must be* stored at <30 °C / <60 %RH and the product *should be* used within 168 hours after opening.
- When the color of the indicator in the packing is changed, the product *should be* baked before soldering.
  - **Baking condition:** 125 +5/-0 °C, 24 hours, 1 time

The products must be baked on the heat-resistant tray because the material (Base Tape, Reel Tape and Cover Tape) is not heat-resistant.

18.2 Handling Conditions

Be careful while handling or transporting products because excessive stress or mechanical shock may break the products.

Handle with care if you suspect that products may have cracks or damages on their terminals. If there is any such damage, the characteristics of products may change. *Do not touch* products with bare hands as that may cause poor solderability and cause damage by static electrical charge.

18.3 Standard PCB Design (Land Pattern and Dimensions)

All the ground terminals should be connected to the ground patterns. Furthermore, the ground pattern should be provided between IN and OUT terminals. Please refer to the specifications for the standard land dimensions.

The recommended land pattern and dimensions should be as per Murata's standard. The characteristics of products may vary depending on the pattern drawing method, grounding method, land dimensions, land forming method of the NC terminals and the PCB material and thickness. Therefore, be sure to verify the characteristics in the actual set.

When using non-standard lands, contact Murata in advance.

18.4 Notice for Chip Placer

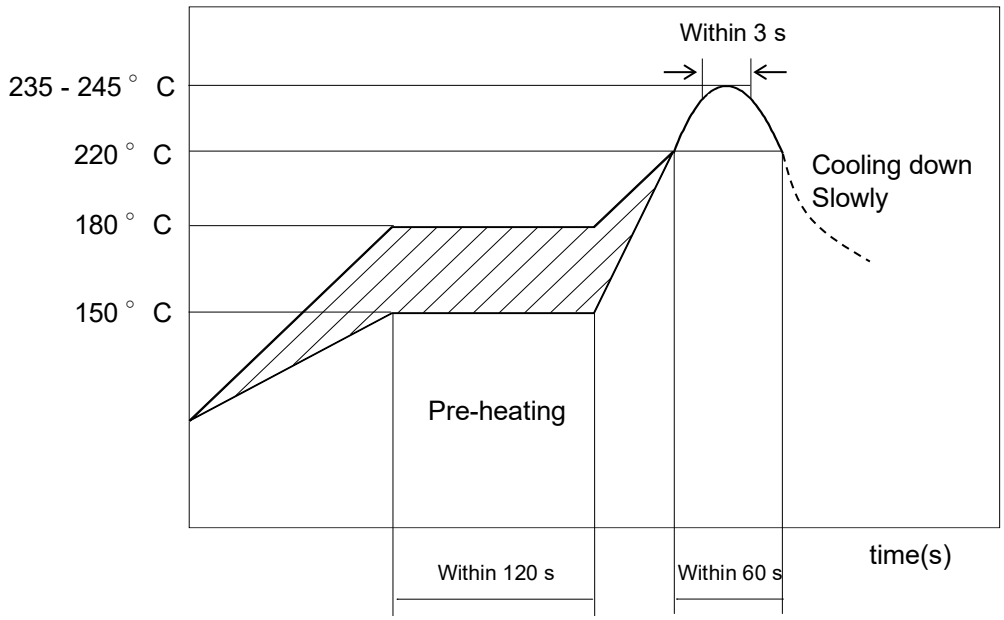
When placing products on the PCB, products may be stressed and broken by uneven forces from a worn-out chucking locating claw or a suction nozzle. To prevent products from damages, be sure to follow the specifications for the maintenance of the chip placer being used. For the positioning of products on the PCB, be aware that mechanical chucking may damage products.

18.5 Soldering Conditions

The recommendation conditions of soldering are as in **Figure 31**.

Soldering must be carried out by the above-mentioned conditions to prevent products damage. Set up the highest temperature of reflow within 260 °C. Contact Murata before use concerning other soldering conditions.

Figure 31: Reflow Soldering Standard Conditions (Example)



- Please use the reflow within 2 times.
- Use rosin type flux or weakly active flux with a chlorine content of 0.2 wt. % or less.

18.6 Cleaning

Since this Product is Moisture Sensitive, cleaning is not recommended. If any cleaning process is done the customer is responsible for any issues or failures caused such process.

18.7 Operational Environment Conditions

Murata products are designed to work for electronic products under normal environmental conditions (ambient temperature, humidity, and pressure). Therefore, there is no problem in using the products under the above-mentioned conditions. However, using the products under the following circumstances may damage products and cause electricity leakage and abnormal temperature may occur:

- In atmosphere containing corrosive gas (Cl_2, NH_3, SO_X, NO_X etc.).
- In atmosphere containing combustible and volatile gases.
- Dusty place.
- Direct sunlight place.
- Water splashing place.
- Humid place where water condenses.
- Freezing place.

If there is any chance of using the products under the conditions listed above, consult with Murata before actual use.

Do not apply static electricity or excessive voltage while assembling and measuring the products, as it might be a cause of degradation or destruction to apply static electricity to products.

18.8 Input Power Capacity

Products shall be used in the input power capacity as specified in this specification.

Inform Murata beforehand, in case that the components are used beyond such input power capacity range.

19 Preconditions to Use Our Products

PLEASE READ THIS NOTICE BEFORE USING OUR PRODUCTS.

Please make sure that your product has been evaluated and confirmed from the aspect of the fitness for the specifications of our product when our product is mounted to your product.

All the items and parameters in this product specification/datasheet/catalog have been prescribed on the premise that our product is used for the purpose, under the condition and in the environment specified in this specification. You are requested not to use our product deviating from the condition and the environment specified in this specification.

Please note that the only warranty that we provide regarding the products is its conformance to the specifications provided herein. Accordingly, we shall not be responsible for any defects in products or equipment incorporating such products, which are caused under the conditions other than those specified in this specification.

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The product shall not be used in any application listed below which requires especially high reliability for the prevention of such defect as may directly cause damage to the third party's life, body or property. You acknowledge and agree that, if you use our products in such applications, we will not be responsible for any failure to meet such requirements. Furthermore, YOU AGREE TO INDEMNIFY AND DEFEND US AND OUR AFFILIATES AGAINST ALL CLAIMS, DAMAGES, COSTS, AND EXPENSES THAT MAY BE INCURRED, INCLUDING WITHOUT LIMITATION, ATTORNEY FEES AND COSTS, DUE TO THE USE OF OUR PRODUCTS AND THE SOFTWARE IN SUCH APPLICATIONS.

- Aircraft equipment.
- Aerospace equipment.
- Undersea equipment.
- Power plant control equipment.
- Medical equipment.
- Traffic signal equipment.

- Burning / explosion control equipment.
- Disaster prevention / crime prevention equipment.
- Transportation equipment (vehicles, trains, ships, elevator, etc.).
- Application of similar complexity and/ or reliability requirements to the applications listed in the above.

We expressly prohibit you from analyzing, breaking, reverse-engineering, remodeling altering, and reproducing our product. Our product cannot be used for the product which is prohibited from being manufactured, used, and sold by the regulations and laws in the world.

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Please do not use our products, our technical information and other data provided by us for the purpose of developing of mass-destruction weapons and the purpose of military use.

Moreover, you must comply with "foreign exchange and foreign trade law", the "U.S. export administration regulations", etc.

Please note that we may discontinue the manufacture of our products, due to reasons such as end of supply of materials and/or components from our suppliers.

By signing on specification sheet or approval sheet, you acknowledge that you are the legal representative for your company and that you understand and accept the validity of the contents herein. When you are not able to return the signed version of specification sheet or approval sheet within 30 days from receiving date of specification sheet or approval sheet, it shall be deemed to be your consent on the content of specification sheet or approval sheet. Customer acknowledges that engineering samples may deviate from specifications and may contain defects due to their development status. We reject any liability or product warranty for engineering samples. In particular we disclaim liability for damages caused by

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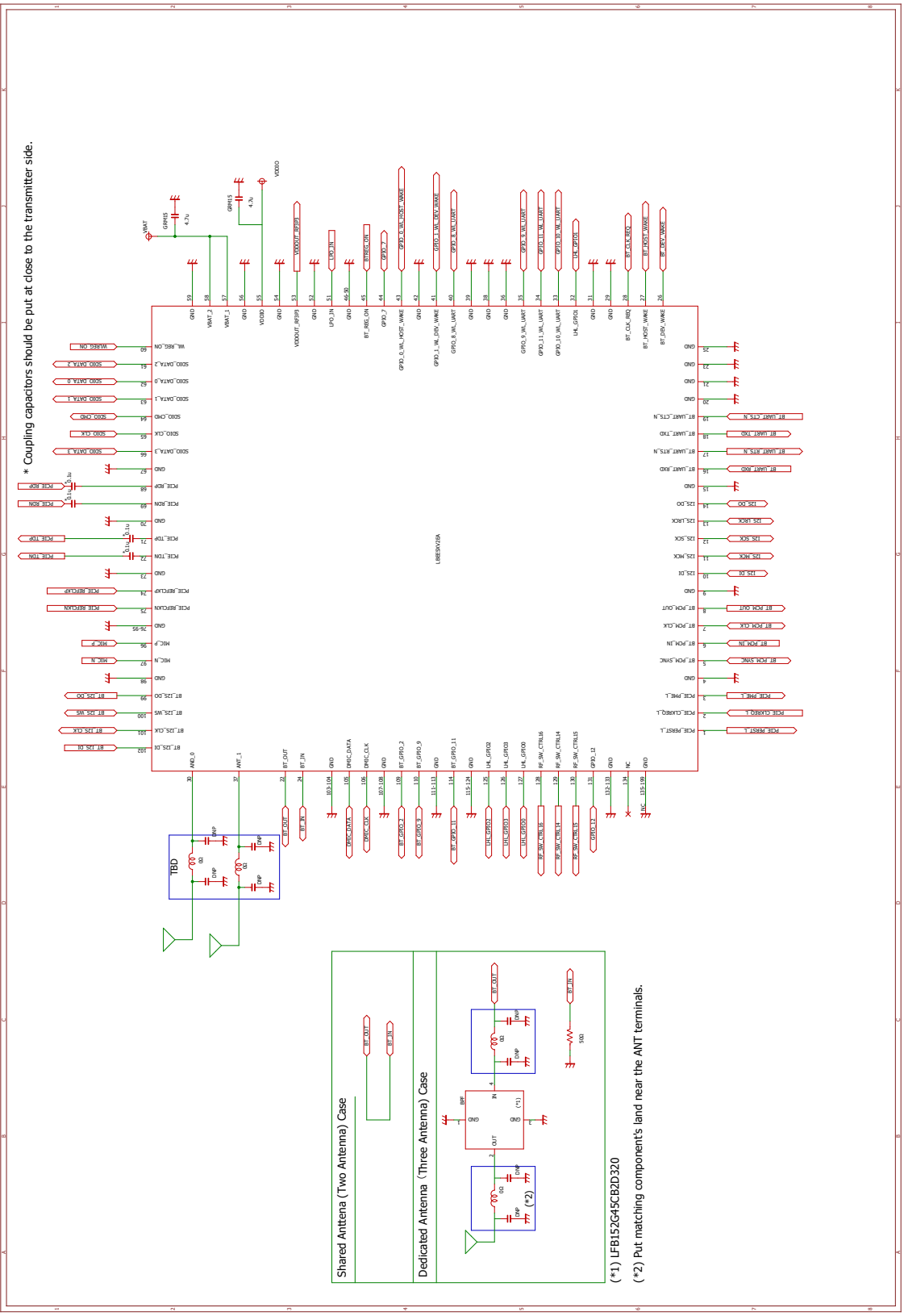
- Deviation or lapse in function of engineering sample,
- Improper use of engineering samples.

We disclaim any liability for consequential and incidental damages.

If you can’t agree with the above contents, please contact sales.

Appendix

Reference circuit


* Coupling capacitors should be put at close to the transmitter side.
TBD
Shared Antenna (Two Antenna) Case
Dedicated Antenna (Three Antenna) Case
(*1) LFB152G45CB2D320
(*2) Put matching component's land near the ANT terminals.

Revision History

Revision Code	Date	Changed Item	Comment
	Aug 20, 2021	First issue	
A	Sep 13, 2021	3. Block Diagram	• Updated
B	Sep 24, 2021	2. KEY FEATURE 5. OPERATING CONDITION 7. DIMENSIONS, MARKING AND TERMINAL CONFIGURATIONS 8. MODULE PIN DESCRIPTIONS 9. REFERENCE PERIPHERAL CIRCUIT 11.1. POWER ON SEQUENCE 11.2. POWER OFF SEQUENCE 12.1. Bluetooth UART Timing 12.3. Bluetooth I2S Interface Timing	• Updated • Changed Operating Temperature • Updated • Updated • Updated • Updated and Revised • Removed • Corrected • Corrected
C	Dec 14, 2021	2. Key Feature 5. Operating Condition 10. Strapping Options 11. I/O Status	• Updated • Added Specification Temperature • Added • Added
D	Apr 05, 2022	Cover Page 1. Scope 14. ELECTICAL CHARACTERISTICS 16. TAPE AND REEL PACKING	• Updated Bluetooth version • Updated Bluetooth version • Updated Tx Power Level and etc. • Updated Dimensions of Tape (Plastic Tape)
E	Dec 10, 2022	2. Key Features 3. Block Diagram 9. Reference Peripheral Circuit 14. Electorical Characteristics	• Updated information. • Created section ‘Ordering Information’. • Moved section to HW app note. • Renamed section Updated to new format
F	June 08, 2023	2. Key Features 3 Ordering Information 6.1 Module Pin Layout (Top View) 6.2 Pin Descriptions 8 Operating Condition 11 I/O State 13.4 WLAN SDIO Timing 13.5 PCI Express Interface Parameters 14. Electrical Characteristics 16 Radio Regulatory Certification by Country for LBEE5XV2EA	• Updated information. • Updated information. • Updated pin name following IC datasheet • Updated pin name following IC datasheet • Added ‘Peak Current’ • Updated information. • Added • Added • Updated information. • Added